

## Virtex-5 Electrical Characteristics

Virtex™-5 FPGAs are available in -3, -2, -1 speed grades, with -3 having the highest performance.

Virtex-5 DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Virtex-5 data sheet, part of an overall set of documentation on the Virtex-5 family of FPGAs, is available on the Xilinx website:

- Virtex-5 Family Overview
- Virtex-5 User Guide
- Virtex-5 Configuration Guide
- Virtex-5 XtremeDSP™ Design Considerations
- Virtex-5 Packaging and Pinout Specification
- Virtex-5 RocketIO™ GTP Transceiver User Guide
- Virtex-5 Tri-mode Ethernet MAC User Guide
- Virtex-5 Integrated Endpoint Block User Guide for PCI Express® Designs
- Virtex-5 System Monitor User Guide
- Virtex-5 PCB Designer's Guide

All specifications are subject to change without notice.

## Virtex-5 DC Characteristics

Table 1: Absolute Maximum Ratings

Symbol	Description		Units
$V_{CCINT}$	Internal supply voltage relative to GND	-0.5 to 1.1	V
$V_{CCAUX}$	Auxiliary supply voltage relative to GND	-0.5 to 3.0	V
$V_{CCO}$	Output drivers supply voltage relative to GND	-0.5 to 3.75	V
$V_{BATT}$	Key memory battery backup supply	-0.5 to 4.05	V
$V_{REF}$	Input reference voltage	-0.5 to 3.75	V
$V_{IN}^{(3)}$	3.3V I/O input voltage relative to GND <sup>(4)</sup> (user and dedicated I/Os)	-0.75 to 4.05	V
	2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)	-0.75 to $V_{CCO} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state 3.3V output <sup>(4)</sup> (user and dedicated I/Os)	-0.75 to 4.05	V
	Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os)	-0.75 to $V_{CCO} + 0.5$	V
$T_{STG}$	Storage temperature (ambient)	-65 to 150	°C
$T_{SOL}$	Maximum soldering temperature <sup>(2)</sup>	+220	°C
$T_J$	Maximum junction temperature <sup>(2)</sup>	+125	°C

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For soldering guidelines and thermal considerations, see [UG195: Virtex-5 Packaging and Pinout Specification](#) on the Xilinx website.
3. 3.3V I/O absolute maximum limit applied to DC and AC signals.
4. For 3.3V I/O operation, refer to [UG190: Virtex-5 User Guide, Chapter 6, 3.3V I/O Design Guidelines](#).

**Table 2: Recommended Operating Conditions**

Symbol	Description	Temperature Range	Min	Max	Units
$V_{CCINT}$	Internal supply voltage relative to GND, $T_J = 0^\circ\text{C}$ to $+85^\circ\text{C}$	Commercial	0.95	1.05	V
	Internal supply voltage relative to GND, $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$	Industrial	0.95	1.05	V
$V_{CCAUX}^{(1)}$	Auxiliary supply voltage relative to GND, $T_J = 0^\circ\text{C}$ to $+85^\circ\text{C}$	Commercial	2.375	2.625	V
	Auxiliary supply voltage relative to GND, $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$	Industrial	2.375	2.625	V
$V_{CCO}^{(2,4,5)}$	Supply voltage relative to GND, $T_J = 0^\circ\text{C}$ to $+85^\circ\text{C}$	Commercial	1.14	3.45	V
	Supply voltage relative to GND, $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$	Industrial	1.14	3.45	V
$V_{IN}$	3.3V supply voltage relative to GND, $T_J = 0^\circ\text{C}$ to $+85^\circ\text{C}$	Commercial	GND – 0.20	3.45	V
	3.3V supply voltage relative to GND, $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$	Industrial	GND – 0.20	3.45	V
	2.5V and below supply voltage relative to GND, $T_J = 0^\circ\text{C}$ to $+85^\circ\text{C}$	Commercial	GND – 0.20	$V_{CCO} + 0.2$	V
	2.5V and below supply voltage relative to GND, $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$	Industrial	GND – 0.20	$V_{CCO} + 0.2$	V
$I_{IN}$	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	Commercial		10	mA
		Industrial		10	mA
$V_{BATT}^{(3)}$	Battery voltage relative to GND, $T_J = 0^\circ\text{C}$ to $+85^\circ\text{C}$	Commercial	1.0	3.6	V
	Battery voltage relative to GND, $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$	Industrial	1.0	3.6	V

**Notes:**

1. Recommended maximum voltage drop for  $V_{CCAUX}$  is 10 mV/ms.
2. Configuration data is retained even if  $V_{CCO}$  drops to 0V.
3.  $V_{BATT}$  is required only when using bitstream encryption. If battery is not used, connect  $V_{BATT}$  to either ground or  $V_{CCAUX}$ .
4. Includes  $V_{CCO}$  of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The configuration supply voltage  $V_{CC\_CONFIG}$  is also known as  $V_{CCO\_0}$

**Table 3: DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Data Rate	Min	Typ	Max	Units
$V_{DRINT}$	Data retention $V_{CCINT}$ voltage (below which configuration data might be lost)		0.75			V
$V_{DRI}$	Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost)		2.0			V
$I_{REF}$	$V_{REF}$ leakage current per pin				10	$\mu\text{A}$
$I_L$	Input or output leakage current per pin (sample-tested)				10	$\mu\text{A}$
$C_{IN}$	Input capacitance (sample-tested)				8	pF
$I_{RPU}^{(1)}$	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 3.3\text{V}$		20		150	$\mu\text{A}$
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 2.5\text{V}$		10		90	$\mu\text{A}$
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 1.8\text{V}$		5		45	$\mu\text{A}$
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 1.5\text{V}$		3		30	$\mu\text{A}$
	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ , $V_{CCO} = 1.2\text{V}$		2		15	$\mu\text{A}$
$I_{RPD}^{(1)}$	Pad pull-down (when selected) @ $V_{IN} = 2.5\text{V}$		5		110	$\mu\text{A}$
$I_{BATT}^{(2)}$	Battery supply current				150	nA
n	Temperature diode ideality factor			1.0002		n
r	Series resistance			5.0		$\Omega$

**Notes:**

1. Typical values are specified at nominal voltage,  $25^\circ\text{C}$ .
2. Maximum value specified for worst case process at  $25^\circ\text{C}$ .

### Important Note

Typical values for quiescent supply current are now specified at nominal voltage, 85°C junction temperatures ( $T_j$ ). Xilinx recommends analyzing static power consumption at  $T_j = 85^\circ\text{C}$  because the majority of designs operate near the high end of the commercial temperature range. Data sheets for older products (e.g., Virtex-4 devices) still specify typical quiescent supply current at  $T_j = 25^\circ\text{C}$ . Quiescent supply current is specified by speed grade for Virtex-5 devices. Use the XPOWER™ Estimator (XPE) spreadsheet tool (download at <http://www.xilinx.com/power>) to calculate static power consumption for conditions other than those specified in Table 4.

**Table 4: Typical Quiescent Supply Current**

Symbol	Description	Device	Speed and Temperature Grade			Units
			-3 (C)	-2 (C & I)	-1 (C & I)	
$I_{CCINTQ}$	Quiescent $V_{CCINT}$ supply current	XC5VLX30	480	480	300	mA
		XC5VLX30T	507	507	317	mA
		XC5VLX50	651	651	449	mA
		XC5VLX50T	689	689	475	mA
		XC5VLX85	1072	1072	883	mA
		XC5VLX85T	1115	1115	866	mA
		XC5VLX110	1391	1391	1109	mA
		XC5VLX110T	1448	1448	1154	mA
		XC5VLX220	N/A	2783	2278	mA
		XC5VLX220T	N/A	2844	2328	mA
		XC5VLX330	N/A	4193	3432	mA
		XC5VLX330T	N/A	4267	3492	mA
		XC5VSX35T	720	720	554	mA
		XC5VSX50T	1092	1092	840	mA
		XC5VSX95T	N/A	1924	1475	mA
$I_{CCOQ}$	Quiescent $V_{CCO}$ supply current	XC5VLX30	1.5	1.5	1.5	mA
		XC5VLX30T	1.5	1.5	1.5	mA
		XC5VLX50	2	2	2	mA
		XC5VLX50T	2	2	2	mA
		XC5VLX85	3	3	3	mA
		XC5VLX85T	3	3	3	mA
		XC5VLX110	4	4	4	mA
		XC5VLX110T	4	4	4	mA
		XC5VLX220	N/A	8	8	mA
		XC5VLX220T	N/A	8	8	mA
		XC5VLX330	N/A	12	12	mA
		XC5VLX330T	N/A	12	12	mA
		XC5VSX35T	1.5	1.5	1.5	mA
		XC5VSX50T	2	2	2	mA
		XC5VSX95T	N/A	4	4	mA

Table 4: Typical Quiescent Supply Current (Continued)

Symbol	Description	Device	Speed and Temperature Grade			Units
			-3 (C)	-2 (C & I)	-1 (C & I)	
I <sub>CCAUXQ</sub>	Quiescent V <sub>CCAUX</sub> supply current	XC5VLX30	38	38	38	mA
		XC5VLX30T	43	43	43	mA
		XC5VLX50	57	57	57	mA
		XC5VLX50T	62	62	62	mA
		XC5VLX85	93	93	93	mA
		XC5VLX85T	98	98	98	mA
		XC5VLX110	125	125	125	mA
		XC5VLX110T	130	130	130	mA
		XC5VLX220	N/A	229	229	mA
		XC5VLX220T	N/A	236	236	mA
		XC5VLX330	N/A	345	345	mA
		XC5VLX330T	N/A	353	353	mA
		XC5VSX35T	49	49	49	mA
		XC5VSX50T	74	74	74	mA
		XC5VSX95T	N/A	131	131	mA

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T<sub>j</sub>). Industrial(I) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

## Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The power supplies can be turned on in any sequence, though the specifications shown in Table 5 are for the recommended power-on sequence of V<sub>CCINT</sub>, V<sub>CCAUX</sub>, and V<sub>CCO</sub>. Xilinx does not specify the current for other power-on sequences.

Table 5 shows the minimum current required by Virtex-5 devices for proper power-on and configuration.

If the current minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

The FPGA must be configured after V<sub>CCINT</sub> is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 5: Power-On Current for Virtex-5 Devices

Device	I <sub>CCINTMIN</sub>		I <sub>CCAUXMIN</sub>		I <sub>CCOMIN</sub>		Units
	Typ <sup>(1)</sup>	Max	Typ <sup>(1)</sup>	Max	Typ <sup>(1)</sup>	Max	
XC5VLX30	235		76		50		mA
XC5VLX30T	246		86		50		mA
XC5VLX50	320		114		50		mA
XC5VLX50T	336		124		50		mA
XC5VLX85	492		186		100		mA
XC5VLX85T	515		196		100		mA

**Table 5: Power-On Current for Virtex-5 Devices (Continued)**

Device	I <sub>CCINTMIN</sub>		I <sub>CCAUXMIN</sub>		I <sub>CCOMIN</sub>		Units
	Typ <sup>(1)</sup>	Max	Typ <sup>(1)</sup>	Max	Typ <sup>(1)</sup>	Max	
XC5VLX110	623		250		100		mA
XC5VLX110T	651		260		100		mA
XC5VLX220	1023		458		150		mA
XC5VLX220T	1056		472		150		mA
XC5VLX330	1470		690		150		mA
XC5VLX330T	1509		706		150		mA
XC5VSX35T	307		98		50		mA
XC5VSX50T	472		148		50		mA
XC5VSX95T	804		262		100		mA

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.

**Table 6: Power Supply Ramp Time**

Symbol	Description	Ramp Time	Units
V <sub>CCINT</sub>	Internal supply voltage relative to GND	0.20 to 50.0	ms
V <sub>CCO</sub>	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V <sub>CCAUX</sub>	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

**SelectIO™ DC Input and Output Levels**

Values for V<sub>IL</sub> and V<sub>IH</sub> are recommended input voltages. Values for I<sub>OL</sub> and I<sub>OH</sub> are guaranteed over the recommended operating conditions at the V<sub>OL</sub> and V<sub>OH</sub> test points. Only selected standards are tested. These are cho-

sen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V<sub>CCO</sub> with the respective V<sub>OL</sub> and V<sub>OH</sub> voltage levels shown. Other standards are sample tested.

**Table 7: SelectIO DC Input and Output Levels**

I/O Standard	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub>	V <sub>OH</sub>	I <sub>OL</sub>	I <sub>OH</sub>
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTTL	-0.3	0.8	2.0	3.45	0.4	2.4	Note(3)	Note(3)
LVC MOS33, LVDCI33	-0.3	0.8	2.0	3.45	0.4	V <sub>CCO</sub> - 0.4	Note(3)	Note(3)
LVC MOS25, LVDCI25	-0.3	0.7	1.7	V <sub>CCO</sub> + 0.3	0.4	V <sub>CCO</sub> - 0.4	Note(3)	Note(3)
LVC MOS18, LVDCI18	-0.3	35% V <sub>CCO</sub>	65% V <sub>CCO</sub>	V <sub>CCO</sub> + 0.3	0.45	V <sub>CCO</sub> - 0.45	Note(4)	Note(4)
LVC MOS15, LVDCI15	-0.3	35% V <sub>CCO</sub>	65% V <sub>CCO</sub>	V <sub>CCO</sub> + 0.3	25% V <sub>CCO</sub>	75% V <sub>CCO</sub>	Note(4)	Note(4)
LVC MOS12	-0.3	35% V <sub>CCO</sub>	65% V <sub>CCO</sub>	V <sub>CCO</sub> + 0.3	25% V <sub>CCO</sub>	75% V <sub>CCO</sub>	Note(6)	Note(6)
PCI33_3 <sup>(5)</sup>	-0.2	30% V <sub>CCO</sub>	50% V <sub>CCO</sub>	V <sub>CCO</sub>	10% V <sub>CCO</sub>	90% V <sub>CCO</sub>	Note(5)	Note(5)
PCI66_3 <sup>(5)</sup>	-0.2	30% V <sub>CCO</sub>	50% V <sub>CCO</sub>	V <sub>CCO</sub>	10% V <sub>CCO</sub>	90% V <sub>CCO</sub>	Note(5)	Note(5)
PCI-X <sup>(5)</sup>	-0.2	35% V <sub>CCO</sub>	50% V <sub>CCO</sub>	V <sub>CCO</sub>	10% V <sub>CCO</sub>	90% V <sub>CCO</sub>	Note(5)	Note(5)

**Table 7: SelectIO DC Input and Output Levels (Continued)**

I/O Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
GTLP	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	-	0.6	N/A	36	N/A
GTL	-0.3	$V_{REF} - 0.05$	$V_{REF} + 0.05$	-	0.4	N/A	32	N/A
HSTL I <sub>12</sub>	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	25% $V_{CCO}$	75% $V_{CCO}$	6.3	6.3
HSTL I <sup>(2)</sup>	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	8	-8
HSTL II <sup>(2)</sup>	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	16	-16
HSTL III <sup>(2)</sup>	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	24	-8
HSTL IV <sup>(2)</sup>	-0.3	$V_{REF} - 0.1$	$V_{REF} + 0.1$	$V_{CCO} + 0.3$	0.4	$V_{CCO} - 0.4$	48	-8
DIFF HSTL I <sup>(2)</sup>	-0.3	50% $V_{CCO} - 0.1$	50% $V_{CCO} + 0.1$	$V_{CCO} + 0.3$	-	-	-	-
DIFF HSTL II <sup>(2)</sup>	-0.3	50% $V_{CCO} - 0.1$	50% $V_{CCO} + 0.1$	$V_{CCO} + 0.3$	-	-	-	-
SSTL2 I	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCO} + 0.3$	$V_{TT} - 0.61$	$V_{TT} + 0.61$	8.1	-8.1
SSTL2 II	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCO} + 0.3$	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	-16.2
DIFF SSTL2 I	-0.3	50% $V_{CCO} - 0.15$	50% $V_{CCO} + 0.15$	$V_{CCO} + 0.3$	-	-	-	-
DIFF SSTL2 II	-0.3	50% $V_{CCO} - 0.15$	50% $V_{CCO} + 0.15$	$V_{CCO} + 0.3$	-	-	-	-
SSTL18 I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.3$	$V_{TT} - 0.47$	$V_{TT} + 0.47$	6.7	-6.7
SSTL18 II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.3$	$V_{TT} - 0.60$	$V_{TT} + 0.60$	13.4	-13.4
DIFF SSTL18 I	-0.3	50% $V_{CCO} - 0.125$	50% $V_{CCO} + 0.125$	$V_{CCO} + 0.3$	-	-	-	-
DIFF SSTL18 II	-0.3	50% $V_{CCO} - 0.125$	50% $V_{CCO} + 0.125$	$V_{CCO} + 0.3$	-	-	-	-

**Notes:**

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. For more information on PCI33\_3, PCI66\_3, and PCI-X, refer to refer to [UG190: Virtex-5 User Guide, Chapter 6, 3.3V I/O Design Guidelines](#).
6. Supported drive strengths of 2, 4, 6, or 8 mA.

## HT DC Specifications (HT\_25)

Table 8: HT DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
$V_{CCO}$	Supply Voltage		2.38	2.5	2.63	V
$V_{OD}$	Differential Output Voltage	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	495	600	715	mV
$\Delta V_{OD}$	Change in $V_{OD}$ Magnitude		-15		15	mV
$V_{OCM}$	Output Common Mode Voltage	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	495	600	715	mV
$\Delta V_{OCM}$	Change in $V_{OCM}$ Magnitude		-15		15	mV
$V_{ID}$	Input Differential Voltage		200	600	1000	mV
$\Delta V_{ID}$	Change in $V_{ID}$ Magnitude		-15		15	mV
$V_{ICM}$	Input Common Mode Voltage		440	600	780	mV
$\Delta V_{ICM}$	Change in $V_{ICM}$ Magnitude		-15		15	mV

## LVDS DC Specifications (LVDS\_25)

Table 9: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
$V_{CCO}$	Supply Voltage		2.38	2.5	2.63	V
$V_{OH}$	Output High Voltage for Q and $\bar{Q}$	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals			1.675	V
$V_{OL}$	Output Low Voltage for Q and $\bar{Q}$	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	0.825			V
$V_{ODIFF}$	Differential Output Voltage (Q - $\bar{Q}$ ), Q = High ( $\bar{Q}$ - Q), $\bar{Q}$ = High	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	247	350	600	mV
$V_{OCM}$	Output Common-Mode Voltage	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	1.125	1.250	1.375	V
$V_{IDIFF}$	Differential Input Voltage (Q - $\bar{Q}$ ), Q = High ( $\bar{Q}$ - Q), $\bar{Q}$ = High		100	350	600	mV
$V_{ICM}$	Input Common-Mode Voltage		0.3	1.2	2.2	V

## Extended LVDS DC Specifications (LVDS\_EXT\_25)

Table 10: Extended LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
$V_{CCO}$	Supply Voltage		2.38	2.5	2.63	V
$V_{OH}$	Output High Voltage for Q and $\bar{Q}$	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals		-	1.785	V
$V_{OL}$	Output Low Voltage for Q and $\bar{Q}$	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	0.715	-	-	V
$V_{ODIFF}$	Differential Output Voltage (Q - $\bar{Q}$ ), Q = High ( $\bar{Q}$ - Q), $\bar{Q}$ = High	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	350	-	820	mV
$V_{OCM}$	Output Common-Mode Voltage	$R_T = 100 \Omega$ across Q and $\bar{Q}$ signals	1.125	1.250	1.375	V
$V_{IDIFF}$	Differential Input Voltage (Q - $\bar{Q}$ ), Q = High ( $\bar{Q}$ - Q), $\bar{Q}$ = High	Common-mode input voltage = 1.25V	100	-	1000	mV
$V_{ICM}$	Input Common-Mode Voltage	Differential input voltage = $\pm 350$ mV	0.3	1.2	2.2	V

## LVPECL DC Specifications (LVPECL\_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The  $V_{OH}$  levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower com-

mon-mode ranges. Table 11 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see [UG190: Virtex-5 User Guide, Chapter 6, SelectIO Resources](#).

Table 11: LVPECL DC Specifications

Symbol	DC Parameter	Min	Typ	Max	Units
$V_{OH}$	Output High Voltage	$V_{CC} - 1.025$	1.545	$V_{CC} - 0.88$	V
$V_{OL}$	Output Low Voltage	$V_{CC} - 1.81$	0.795	$V_{CC} - 1.62$	V
$V_{ICM}$	Input Common-Mode Voltage	0.6		2.2	V
$V_{IDIFF}$	Differential Input Voltage <sup>(1,2)</sup>	0.100		1.5	V

**Notes:**

1. Recommended input maximum voltage not to exceed  $V_{CCAUX} + 0.2V$ .
2. Recommended input minimum voltage not to go below  $-0.5V$ .



## RocketIO GTP Transceiver Specifications

### RocketIO GTP Transceiver DC Characteristics

**Table 12: Absolute Maximum Ratings**

Symbol	Description		Units
MGTAVCCPLL	Analog supply voltage for the GTP_DUAL shared PLL relative to GND	-0.5 to 1.32	V
MGTAVTTTX	Analog supply voltage for the GTP_DUAL transmitters relative to GND	-0.5 to 1.32	V
MGTAVTTRX	Analog supply voltage for the GTP_DUAL receivers relative to GND	-0.5 to 1.32	V
MGTAVCC	Analog supply voltage for the GTP_DUAL common circuits relative to GND	-0.5 to 1.32	V
MGTAVTTRXC	Analog supply voltage for the resistor calibration circuit of the GTP_DUAL column	-0.5 to 1.32	V

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

**Table 13: Recommended Operating Conditions<sup>(1)(2)</sup>**

Symbol	Description	Min	Max	Units
MGTAVCCPLL <sup>(1)</sup>	Analog supply voltage for the GTP_DUAL shared PLL relative to GND	1.14	1.26	V
MGTAVTTTX <sup>(1)</sup>	Analog supply voltage for the GTP_DUAL transmitters relative to GND	1.14	1.26	V
MGTAVTTRX <sup>(1)</sup>	Analog supply voltage for the GTP_DUAL receivers relative to GND	1.14	1.26	V
MGTAVCC <sup>(1)</sup>	Analog supply voltage for the GTP_DUAL common circuits relative to GND	0.95	1.05	V
MGTAVTTRXC <sup>(1)</sup>	Analog supply voltage for the resistor calibration circuit of the GTP_DUAL column	1.14	1.26	V

**Notes:**

- Each voltage listed requires the filter circuit described in [UG196: Virtex-5 RocketIO GTP Transceiver User Guide](#).
- Voltages are specified for the temperature range of  $T_J = -40^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ .

**Table 14: DC Characteristics Over Recommended Operating Conditions<sup>(2)</sup>**

Symbol	Description	Min	Typ	Max	Units
$I_{\text{MGTAVTTTX}}$	GTP_DUAL tile transmitter termination supply current <sup>(3)</sup>		71	90	mA
$I_{\text{MGTAVCCPLL}}$	GTP_DUAL tile shared PLL supply current		36	60	mA
$I_{\text{MGTAVTTRXC}}$	GTP_DUAL tile resistor termination calibration supply current		0.1	0.5	mA
$I_{\text{MGTAVTTRX}}$	GTP_DUAL tile receiver termination supply current <sup>(3)</sup>		0.1	0.5	mA
$I_{\text{MGTAVCC}}$	GTP_DUAL tile internal analog supply current		56	110	mA
$R_{\text{REF}}$	Precision reference resistor for internal calibration termination	49.5	50	50.5	$\Omega$

**Notes:**

- Typical values are specified at nominal voltage,  $25^{\circ}\text{C}$ , with a 3.2 Gb/s line rate.
- $I_{\text{CC}}$  numbers are given per GTP\_DUAL tile with both GTP devices operating with default settings.
- AC coupled TX/RX link.

**Table 15: Quiescent Supply Current**

Symbol	Description	Device	Typ <sup>(1)</sup>	Max	Units
I <sub>CCINTQ</sub>	Quiescent internal supply current	XC5VLX30T			mA
		XC5VLX50T			mA
		XC5VLX85T			mA
		XC5VLX110T			mA
		XC5VLX220T			mA
		XC5VLX330T			mA
		XC5VSX35T			mA
		XC5VSX50T			mA
		XC5VSX95T			mA
I <sub>VTTTXQ</sub>	Quiescent transmitter supply current	XC5VLX30T			mA
		XC5VLX50T			mA
		XC5VLX85T			mA
		XC5VLX110T			mA
		XC5VLX220T			mA
		XC5VLX330T			mA
		XC5VSX35T			mA
		XC5VSX50T			mA
		XC5VSX95T			mA
I <sub>AVCCPLLQ</sub>	Quiescent GTP_DUAL PLL supply current	XC5VLX30T			mA
		XC5VLX50T			mA
		XC5VLX85T			mA
		XC5VLX110T			mA
		XC5VLX220T			mA
		XC5VLX330T			mA
		XC5VSX35T			mA
		XC5VSX50T			mA
		XC5VSX95T			mA
I <sub>VTRXCQ</sub>	Quiescent receiver termination switching supply current	XC5VLX30T			mA
		XC5VLX50T			mA
		XC5VLX85T			mA
		XC5VLX110T			mA
		XC5VLX220T			mA
		XC5VLX330T			mA
		XC5VSX35T			mA
		XC5VSX50T			mA
		XC5VSX95T			mA

Table 15: Quiescent Supply Current (Continued)

Symbol	Description	Device	Typ <sup>(1)</sup>	Max	Units
I <sub>TRXQ</sub>	Quiescent receiver termination supply current	XC5VLX30T			mA
		XC5VLX50T			mA
		XC5VLX85T			mA
		XC5VLX110T			mA
		XC5VLX220T			mA
		XC5VLX330T			mA
		XC5VSX35T			mA
		XC5VSX50T			mA
		XC5VSX95T			mA
I <sub>VCCQ</sub>	Quiescent internal analog supply current	XC5VLX30T			mA
		XC5VLX50T			mA
		XC5VLX85T			mA
		XC5VLX110T			mA
		XC5VLX220T			mA
		XC5VLX330T			mA
		XC5VSX35T			mA
		XC5VSX50T			mA
		XC5VSX95T			mA

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. Given for entire die. Powered and unconfigured.
3. Unconnected (if channel is driven to voltage).
4. More accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

### RocketIO GTP Transceiver DC Input and Output Levels

Table 16 summarizes the DC output specifications of the Virtex-5 RocketIO GTP Transceivers. Figure 1 shows the single-ended output voltage swing. Figure 2 shows the peak-to-peak differential output voltage. Consult UG196: Virtex-5 RocketIO GTP Transceiver User Guide for further details.

Table 16: GTP Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV <sub>PPIN</sub>	Differential peak-to-peak input voltage	External AC coupled ≤ 3.2 Gb/s	150		2000	mV
		External AC coupled > 3.2 Gb/s	180		2000	mV
V <sub>IN</sub>	Absolute input voltage	DC coupled MGTAVTTRX = 1.2V	-400		1200	mV
V <sub>CMIN</sub>	Common mode input voltage	DC coupled MGTAVTTRX = 1.2V		800		mV
DV <sub>PPOUT</sub>	Differential peak-to-peak output voltage <sup>(1)</sup>	TXBUFDIFFCTRL = 000, TX_DIFF_BOOST = ON			1400	mV
V <sub>SEOUT</sub>	Single-ended output voltage swing <sup>(1)</sup>	TXBUFDIFFCTRL = 000, TX_DIFF_BOOST = ON			700	mV
V <sub>CMOUT</sub>	Common mode output voltage	Equation based MGTAVTTX = 1.2V	1200 – Amplitude/2			mV
R <sub>IN</sub>	Differential input resistance		90	100	120	Ω
R <sub>OUT</sub>	Differential output resistance		90	100	120	Ω
T <sub>OSKEW</sub>	Transmitter output skew				15	ps
C <sub>EXT</sub>	Recommended external AC coupling capacitor <sup>(2)</sup>		75	100	200	nF

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in UG196: Virtex-5 RocketIO GTP Transceiver User Guide and can result in values lower than reported in this table.
2. Values outside of this range can be used as appropriate to conform to specific protocols and standards.

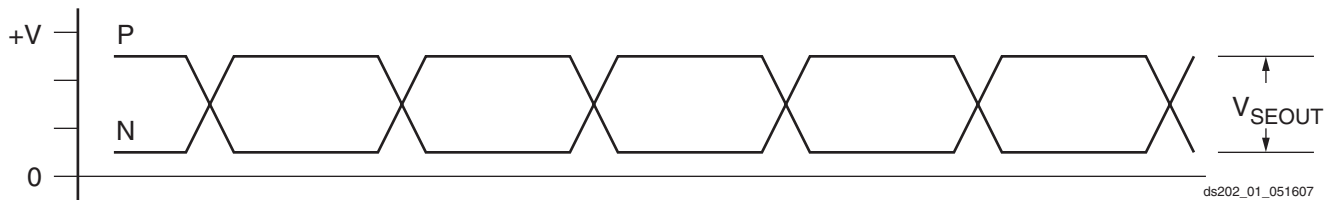


Figure 1: Single-Ended Output Voltage Swing

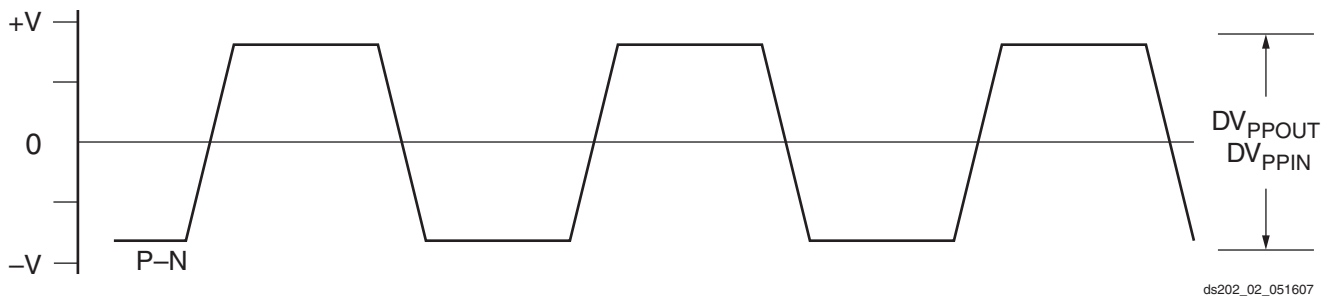


Figure 2: Peak-to-Peak Differential Output Voltage

Table 17 summarizes the DC input specifications of the Virtex-5 RocketIO GTP Transceivers. Figure 3 shows the single-ended input voltage swing. Figure 4 shows the

peak-to-peak differential clock input voltage swing. Consult UG196: Virtex-5 RocketIO GTP Transceiver User Guide for further details.

Table 17: RocketIO GTP Clock DC Input Level Specification<sup>(1)</sup>

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
$DV_{PPIN}$	Differential peak-to-peak input voltage		200	800	2000	mV
$V_{SEIN}$	Single-ended input voltage		100	400	1000	mV
$R_{IN}$	Differential input resistance		80	105	130	$\Omega$
$C_{EXT}$	Required external AC coupling capacitor		75	100	200	nF

Notes:

- $V_{MIN} = 0V$  and  $V_{MAX} = 1200mV$

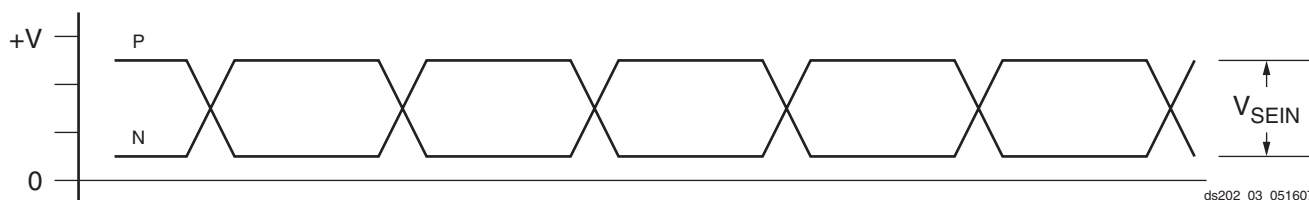


Figure 3: Single-Ended Clock Input Voltage Swing Peak-to-Peak

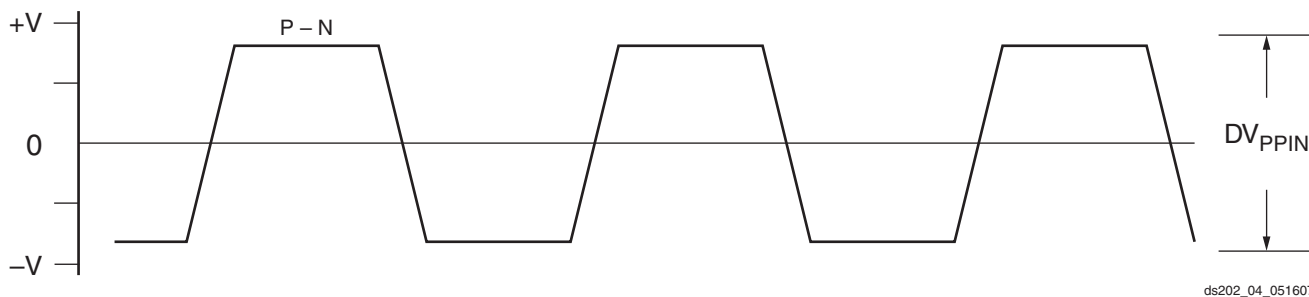


Figure 4: Differential Clock Input Voltage Swing Peak-to-Peak

### RocketIO GTP Switching Characteristics

Consult [UG196](#): *Virtex-5 RocketIO GTP Transceiver User Guide* for further information.

Table 18: GTP Transceiver Performance

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F <sub>GTPMAX</sub>	Maximum GTP transceiver data rate	3.75	3.75	3.2	Gb/s
F <sub>GPLLMAX</sub>	Maximum PLL frequency	2.0	2.0	2.0	GHz
F <sub>GPLLMIN</sub>	Minimum PLL frequency	1.0	1.0	1.0	GHz

Table 19: CRC Block Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F <sub>CRC</sub>	CRCCLK maximum frequency	320	320	250	MHz

Table 20: GTP Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F <sub>GCLK</sub>	Reference clock frequency range <sup>(1)</sup>	CLK	60		350	MHz
T <sub>RCLK</sub>	Reference clock rise time	20% – 80%		200	400	ps
T <sub>FCLK</sub>	Reference clock fall time	80% – 20%		200	400	ps
T <sub>DCREF</sub>	Reference clock duty cycle	CLK	45	50	55	%
T <sub>GJTT</sub>	Reference clock total jitter, peak-peak <sup>(2)</sup>	CLK			40	ps
T <sub>LOCK</sub>	Clock recovery frequency acquisition time	Initial PLL lock			1	ms
T <sub>PHASE</sub>	Clock recovery phase acquisition time	Lock to data after PLL has relocked to the reference clock. Includes lock to reference time.			200	µs

**Notes:**

1. The clock from the GTP\_DUAL differential clock pin pair can be used for all serial bit rates. GREFCLK can be used for serial bit rates up to 1 Gb/s.
2. Measured at the package pin.

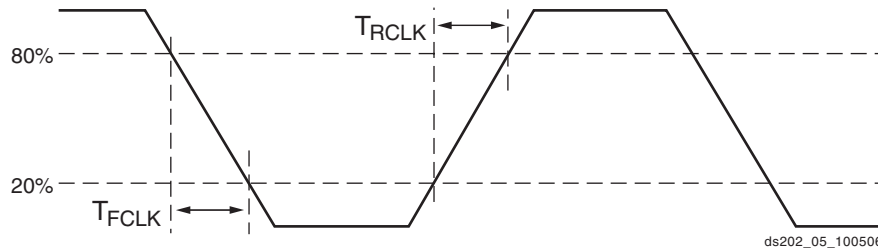


Figure 5: Reference Clock Timing Parameters

**Table 21: GTP User Clock Switching Characteristics<sup>(1)</sup>**

Symbol	Description	Conditions	Speed Grade			Units
			-3	-2	-1	
F <sub>TXOUT</sub>	TXOUTCLK maximum frequency		375	375	320	MHz
F <sub>RXREC</sub>	RXRECCLK maximum frequency		375	375	320	MHz
T <sub>RX</sub>	RXUSRCLK maximum frequency		375	375	320	MHz
T <sub>RX2</sub>	RXUSRCLK2 maximum frequency	RXDATAWIDTH = 0	350	350	320	MHz
		RXDATAWIDTH = 1	187.5	187.5	160	MHz
T <sub>TX</sub>	TXUSRCLK maximum frequency		375	375	320	MHz
T <sub>TX2</sub>	TXUSRCLK2 maximum frequency	TXDATAWIDTH = 0	350	350	320	MHz
		TXDATAWIDTH = 1	187.5	187.5	160	MHz

**Notes:**

1. Clocking must be implemented as described in [UG196: Virtex-5 RocketIO GTP Transceiver User Guide](#)

**Table 22: GTP Transmitter Switching Characteristics**

Symbol	Description	Min	Typ	Max	Units
F <sub>GTX</sub>	Serial data rate range	0.1		F <sub>GTPMAX</sub>	Gb/s
T <sub>RTX</sub>	TX Rise time		140		ps
T <sub>FTX</sub>	TX Fall time		120		ps
T <sub>LLSKEW</sub>	TX lane-to-lane skew <sup>(1)</sup>			2 + 500 ps	UI
V <sub>TXOVBVDDP</sub>	Electrical idle amplitude			20	mV
T <sub>TXOVBTRANS</sub>	Electrical idle transition time			40	ns
T <sub>J3.75</sub>	Total Jitter <sup>(2)</sup>			0.35	UI
D <sub>J3.75</sub>	Deterministic Jitter <sup>(2)</sup>			0.19	UI
T <sub>J3.2</sub>	Total Jitter <sup>(2)</sup>			0.35	UI
D <sub>J3.2</sub>	Deterministic Jitter <sup>(2)</sup>			0.19	UI
T <sub>J2.5</sub>	Total Jitter <sup>(2)</sup>			0.30	UI
D <sub>J2.5</sub>	Deterministic Jitter <sup>(2)</sup>			0.14	UI
T <sub>J2.0</sub>	Total Jitter <sup>(2)</sup>			0.30	UI
D <sub>J2.0</sub>	Deterministic Jitter <sup>(2)</sup>			0.14	UI
T <sub>J1.25</sub>	Total Jitter <sup>(2)</sup>			0.20	UI
D <sub>J1.25</sub>	Deterministic Jitter <sup>(2)</sup>			0.10	UI
T <sub>J1.00</sub>	Total Jitter <sup>(2)</sup>			0.20	UI
D <sub>J1.00</sub>	Deterministic Jitter <sup>(2)</sup>			0.10	UI
T <sub>J500</sub>	Total Jitter <sup>(2)</sup>			0.10	UI
D <sub>J500</sub>	Deterministic Jitter <sup>(2)</sup>			0.04	UI
T <sub>J100</sub>	Total Jitter <sup>(2)</sup>			0.02	UI
D <sub>J100</sub>	Deterministic Jitter <sup>(2)</sup>			0.01	UI

**Notes:**

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP\_DUAL sites.
2. Using PLL\_DIVSEL\_FB = 2, INTDATAWIDTH = 1.
3. All jitter values are based on a Bit-Error Ratio of 1e<sup>-12</sup>.

**Table 23: GTP Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F <sub>GRX</sub>	Serial data rate	RX oversampler not enabled	0.5		F <sub>GTPMAX</sub>	Gb/s
		RX oversampler enabled	0.1		0.5	Gb/s
R <sub>XOOBVDPP</sub>	OOB detect threshold peak-to-peak	OOBDETECT_THRESHOLD = 100	60	105	165	mV
R <sub>XSST</sub>	Receiver spread-spectrum tracking <sup>(1)</sup>	Modulated @ 33 KHz	-5000		0	ppm
R <sub>XRL</sub>	Run length (CID)	Internal AC capacitor bypassed			150	UI
R <sub>XPPMTOL</sub>	Data/REFCLK PPM offset tolerance	ACDR 2 <sup>nd</sup> -order loop enabled	-1000		1000	ppm
<b>SJ Jitter Tolerance</b>						
JT_SJ <sub>3.75</sub>	Sinusoidal Jitter <sup>(2)</sup>	3.75 Gb/s	0.30			UI
JT_SJ <sub>3.2</sub>	Sinusoidal Jitter <sup>(2)</sup>	3.20 Gb/s	0.40			UI
JT_SJ <sub>2.50</sub>	Sinusoidal Jitter <sup>(2)</sup>	2.50 Gb/s	0.40			UI
JT_SJ <sub>2.00</sub>	Sinusoidal Jitter <sup>(2)</sup>	2.00 Gb/s	0.40			UI
JT_SJ <sub>1.00</sub>	Sinusoidal Jitter <sup>(2)</sup>	1.00 Gb/s	0.30			UI
JT_SJ <sub>500</sub>	Sinusoidal Jitter <sup>(2)</sup>	500 Mb/s	0.30			UI
JT_SJ <sub>500</sub>	Sinusoidal Jitter <sup>(2)</sup>	500 Mb/s OS	0.30			UI
JT_SJ <sub>100</sub>	Sinusoidal Jitter <sup>(2)</sup>	100 Mb/s OS	0.30			UI
<b>SJ Jitter Tolerance with Stressed Eye</b>						
JT_TJSE <sub>3.2</sub>	Total Jitter with Stressed Eye <sup>(3)</sup>	3.20 Gb/s	0.87			UI
JT_SJSE <sub>3.2</sub>	Sinusoidal Jitter with Stressed Eye <sup>(3)</sup>	3.20 Gb/s	0.30			UI

**Notes:**

- Using PLL\_RX\_DIVSEL\_OUT = 1.
- Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
- Stimulus signal includes 0.4UI of DJ and 0.17UI of RJ. RX equalizer is enabled.
- All jitter values are based on a Bit Error Ratio of 1e<sup>-12</sup>.

## Ethernet MAC Switching Characteristics

Consult [UG194: Virtex-5 Tri-mode Ethernet Media Access Controller User Guide](#) for further information.

**Table 24: Maximum Ethernet MAC Performance**

Description	Speed Grade			Units
	-3	-2	-1	
Ethernet MAC Maximum Performance	10/100/1000			Mb/s



## System Monitor Analog-to-Digital Converter Specification

Table 25: Analog-to-Digital Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
$V_{DD} = 2.5V \pm 2\%$ , $V_{REFP} = 2.5V$ , $V_{REFN} = 0V$ , $ADCCLK = 5.2\text{ MHz}$ , $T_A = T_{MIN}$ to $T_{MAX}$ , Typical values at $T_A = +25^\circ\text{C}$						
<b>DC Accuracy:</b> All external input channels such as $V_P/V_N$ and $V_{AUXP}[15:0]/V_{AUXN}[15:0]$ , Unipolar Mode, and Common Mode = 0V						
Resolution			10			Bits
Integral Nonlinearity	INL				$\pm 2$	LSBs
Differential Nonlinearity	DNL	No missing codes ( $T_{MIN}$ to $T_{MAX}$ ) Guaranteed Monotonic			$\pm 0.9$	LSBs
Unipolar Offset Error <sup>(1)</sup>		Uncalibrated		$\pm 2$	$\pm 30$	LSBs
Bipolar Offset Error <sup>(1)</sup>		Uncalibrated measured in bipolar mode		$\pm 2$	$\pm 30$	LSBs
Gain Error <sup>(1)</sup>		Uncalibrated		$\pm 0.2$	$\pm 2$	%
Bipolar Gain Error <sup>(1)</sup>		Uncalibrated measured in bipolar mode		$\pm 0.2$	$\pm 2$	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. $V_{REFP} - V_{REFN} = 2.5V$		$\pm 10$		LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. $V_{REFP} - V_{REFN} = 2.5V$		$\pm 1$	$\pm 2$	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature		$\pm 0.01$		LSB/ $^\circ\text{C}$
DC Common-Mode Reject	CMRR <sub>DC</sub>	$V_N = V_{CM} = 0.5V \pm 0.5V$ , $V_P - V_N = 100\text{mV}$		70		dB
<b>Conversion Rate<sup>(2)</sup></b>						
Conversion Time - Continuous	$t_{CONV}$	Number of CLK cycles	26		32	
Conversion Time - Event	$t_{CONV}$	Number of CLK cycles			21	
T/H Acquisition Time	$t_{ACQ}$	Number of CLK cycles	4			
DRP Clock Frequency	DCLK	DRP clock frequency	8		250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1		5.2	MHz
CLK Duty cycle			40		60	%
<b>Analog Inputs<sup>(3)</sup></b>						
Dedicated Analog Inputs Input Voltage Range $V_P - V_N$		Unipolar Operation	0		1	Volts
		Differential Inputs	-0.25		+0.25	
		Unipolar Common Mode Range (FS input)	0		+0.5	
		Differential Common Mode Range (FS input)	+0.3		+0.7	
			Bandwidth		20	
Auxiliary Analog Inputs Input Voltage Range $V_{AUXP}[0] / V_{AUXN}[0]$ to $V_{AUXP}[15] / V_{AUXN}[15]$		Unipolar Operation	0		1	Volts
		Differential Operation	-0.25		+0.25	
		Unipolar Common Mode Range (FS input)	0		+0.5	
		Differential Common Mode Range (FS input)	+0.3		+0.7	
			Bandwidth		10	
Input Leakage Current		A/D not converting, ADCCLK stopped		$\pm 1.0$		$\mu\text{A}$

Table 25: Analog-to-Digital Specifications (Continued)

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Input Capacitance				10		pF
On-chip Supply Monitor Error		$V_{CCINT}$ and $V_{CCAUX}$ with calibration enabled			$\pm 1.0$	% Reading
On-chip Temperature Monitor Error		$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ with calibration enabled			$\pm 4$	$^{\circ}\text{C}$
<b>External Reference Inputs<sup>(4)</sup></b>						
Positive Reference Input Voltage Range	$V_{REFP}$	Measured Relative to $V_{REFN}$	2.45	2.5	2.55	Volts
Negative Reference Input Voltage Range	$V_{REFN}$	Measured Relative to AGND	-50	0	100	mV
Input current	$I_{REF}$	ADCCLK = 5.2 MHz			100	$\mu\text{A}$
<b>Power Requirements</b>						
Analog Power Supply	$AV_{DD}$	Measured Relative to $AV_{SS}$	2.45	2.5	2.55	Volts
Analog Supply Current	$AI_{DD}$	ADCCLK = 5.2 MHz	5		8	mA

**Notes:**

- Offset and gain errors are removed by enabling the System Monitor automatic gain calibration feature. See [UG192: Virtex-5 System Monitor User Guide](#).
- See "System Monitor Timing" in [UG192: Virtex-5 System Monitor User Guide](#).
- See "Analog Inputs" in [UG192: Virtex-5 System Monitor User Guide](#) for a detailed description.
- Any variation in the reference voltage from the nominal  $V_{REFP} = 2.5\text{V}$  and  $V_{REFN} = 0\text{V}$  will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing the supply voltage and reference to vary by  $\pm 2\%$  is permitted.

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-5 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the **Switching Characteristics**, page 21. Table 26 shows internal (register-to-register) performance.

Table 26: Register-to-Register Performance

Description	Register-to-Register (with I/O Delays)			Units
	Speed Grade			
	-3	-2	-1	
<b>Basic Functions</b>				
16:1 Multiplexer	550	500	450	MHz
32:1 Multiplexer	550	500	450	MHz
64:1 Multiplexer	511	467	407	MHz
9 x 9 Logic Multiplier with 4 pipe stages	468	438	428	MHz
9 x 9 Logic Multiplier with 5 pipe stages	550	500	428	MHz
16-bit Adder	550	500	450	MHz
32-bit Adder	550	500	447	MHz
64-bit Adder	423	377	323	MHz
Register to LUT to Register	550	500	450	MHz
16-bit Counter	550	500	450	MHz
32-bit Counter	550	500	450	MHz
64-bit Counter	428	381	333	MHz
<b>Memory</b>				
Cascaded block RAM (64K)	500	450	400	MHz
<b>Block RAM Pipelined</b>				
Single-Port 512 x 36 bits	550	500	450	MHz
Single-Port 4096 x 4 bits	550	500	450	MHz
Dual-Port A: 4096 x 4 bits and B: 1024 x 18 bits	550	500	450	MHz
<b>Distributed RAM</b>				
Single-Port 16 x 8	550	500	450	MHz
Single-Port 32 x 8	550	500	450	MHz
Single-Port 64 x 8	550	500	450	MHz
Dual-Port 16 x 8				MHz
<b>Shift Register Chain</b>				
16-bit	550	500	450	MHz
32-bit	550	500	450	MHz
64-bit	550	500	438	MHz

Table 26: Register-to-Register Performance (Continued)

Description	Register-to-Register (with I/O Delays)			Units
	Speed Grade			
	-3	-2	-1	
<b>Dedicated Arithmetic Logic</b>				
DSP48E Quad 12-bit Adder/Subtractor	550	500	450	MHz
DSP48E Dual 24-bit Adder/Subtractor	550	500	450	MHz
DSP48E 48-bit Adder/Subtractor	550	500	450	MHz
DSP48E 48-bit Counter	550	500	450	MHz
DSP48E 48-bit Comparator	550	500	450	MHz
DSP48E 25 x 18 bit Pipelined Multiplier	550	500	450	MHz
DSP48E Direct 4-tap FIR Filter Pipelined	510	458	397	MHz
DSP48E Systolic n-tap FIR Filter Pipelined	550	500	450	MHz

**Notes:**

1. Device used is the XC5VLX50T- FF1136

Table 27: Interface Performances

Description	Speed Grade		
	-3	-2	-1
<b>Networking Applications</b>			
SFI-4.1 (SDR LVDS Interface)	710 MHz	710 MHz	645 MHz
SPI-4.2 (DDR LVDS Interface)	1.25 Gb/s	1.0 Gb/s	1.0 Gb/s
<b>Memory Interfaces</b>			
DDR	200 MHz	200 MHz	200 MHz
DDR2	333 MHz	300 MHz	267 MHz
QDR II SRAM	300 MHz	300 MHz	250 MHz
RLDRAM II	333 MHz	300 MHz	250 MHz

## Switching Characteristics

All values represented in this data sheet are based on speed specification version 1.57. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

## Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

**Table 28** correlates the current status of each Virtex-5 device on a per speed grade basis.

*Table 28: Virtex-5 Device Speed Grade Designations*

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC5VLX30			-3, -2, -1
XC5VLX30T			-3, -2, -1
XC5VLX50			-3, -2, -1
XC5VLX50T			-3, -2, -1
XC5VLX85			-3, -2, -1
XC5VLX85T			-3, -2, -1
XC5VLX110			-3, -2, -1
XC5VLX110T			-3, -2, -1
XC5VLX220			-2, -1
XC5VLX220T			-2, -1
XC5VLX330			-2, -1
XC5VLX330T			-2, -1
XC5VSX35T			-3, -2, -1
XC5VSX50T			-3, -2, -1
XC5VSX95T			-2, -1

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-5 devices.

## Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. **Table 29** lists the production released Virtex-5 family member, speed grade, and the corresponding supported speed specification version and ISE software revisions.

**Table 29: Virtex-5 Production Software and Speed Specification Release**

Device	Speed Grade Designations		
	-3	-2	-1
XC5VLX30	ISE 9.2i SP2 v1.56		
XC5VLX30T	ISE 9.2i SP2 v1.56		
XC5VLX50	ISE 9.2i SP2 v1.56	ISE 9.2i SP1 v1.55	
XC5VLX50T	ISE 9.2i SP2 v1.56	ISE 9.2i SP1 v1.55	
XC5VLX85	ISE 9.2i SP2 v1.56	ISE 9.2i SP1 v1.55	
XC5VLX85T	ISE 9.2i SP2 v1.56	ISE 9.2i SP1 v1.55	
XC5VLX110	ISE 9.2i SP2 v1.56		
XC5VLX110T	ISE 9.2i SP2 v1.56		
XC5VLX220	N/A	ISE 9.2i SP3 v1.57	
XC5VLX220T	N/A	ISE 9.2i SP3 v1.57	
XC5VLX330	N/A	ISE 9.2i SP3 v1.57	
XC5VLX330T	N/A	ISE 9.2i SP3 v1.57	
XC5VSX35T	ISE 9.2i SP3 v1.57		
XC5VSX50T	ISE 9.2i SP3 v1.57	ISE 9.2i SP2 v1.56	
XC5VSX95T	N/A	ISE 9.2i SP3 v1.57	

**Notes:**

- Blank entries indicate a device and/or speed grade in advance or preliminary status.

## IOB Pad Input/Output/3-State Switching Characteristics

**Table 30** summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

$T_{IOP1}$  is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

$T_{IOOP}$  is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

$T_{IOTP}$  is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

**Table 31** summarizes the value of  $T_{IOTPHZ}$ .  $T_{IOTPHZ}$  is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

**Table 30: IOB Switching Characteristics**

I/O Standard	$T_{IOP1}$			$T_{IOOP}$			$T_{IOTP}$			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2	-1	-3	-2	-1	-3	-2	-1	
LVDS_25	0.80	0.90	1.06	1.13	1.29	1.44	1.13	1.29	1.44	ns
LVDS_EXT_25	1.01	1.16	1.30	1.17	1.34	1.49	1.17	1.34	1.49	ns
HT_25	0.80	0.90	1.06	1.10	1.26	1.40	1.10	1.26	1.40	ns
BLVDS_25	0.80	0.90	1.06	1.24	1.38	1.58	1.24	1.38	1.58	ns
RSDS_25 (point to point)	0.80	0.90	1.06	1.13	1.29	1.44	1.13	1.29	1.44	ns
ULVDS_25	0.80	0.90	1.06	1.10	1.27	1.41	1.10	1.27	1.41	ns
PCI33_3	0.62	0.70	0.82	1.85	2.06	2.38	1.85	2.06	2.38	ns
PCI66_3	0.62	0.70	0.82	1.85	2.06	2.38	1.85	2.06	2.38	ns
PCI-X	0.62	0.70	0.82	1.40	1.56	1.80	1.40	1.56	1.80	ns
GTL	0.76	0.85	1.00	1.47	1.63	1.86	1.47	1.63	1.86	ns
GTLP	0.76	0.85	1.00	1.51	1.68	1.93	1.51	1.68	1.93	ns
HSTL_I	0.76	0.85	1.00	1.42	1.57	1.79	1.42	1.57	1.79	ns
HSTL_II	0.76	0.85	1.00	1.39	1.53	1.74	1.39	1.53	1.74	ns
HSTL_III	0.76	0.85	1.00	1.44	1.60	1.85	1.44	1.60	1.85	ns
HSTL_IV	0.76	0.85	1.00	1.44	1.60	1.83	1.44	1.60	1.83	ns
HSTL_I_18	0.76	0.85	1.00	1.40	1.55	1.77	1.40	1.55	1.77	ns
HSTL_II_18	0.76	0.85	1.00	1.36	1.51	1.72	1.36	1.51	1.72	ns
HSTL_III_18	0.76	0.85	1.00	1.45	1.61	1.85	1.45	1.61	1.85	ns
HSTL_IV_18	0.76	0.85	1.00	1.41	1.57	1.81	1.41	1.57	1.81	ns
SSTL2_I	0.76	0.85	1.00	1.48	1.64	1.87	1.48	1.64	1.87	ns
SSTL2_II	0.76	0.85	1.00	1.40	1.55	1.76	1.40	1.55	1.76	ns
LVTTTL, Slow, 2 mA	0.62	0.70	0.82	4.10	4.47	5.01	4.10	4.47	5.01	ns
LVTTTL, Slow, 4 mA	0.62	0.70	0.82	2.87	3.09	3.41	2.87	3.09	3.41	ns
LVTTTL, Slow, 6 mA	0.62	0.70	0.82	2.66	2.91	3.29	2.66	2.91	3.29	ns
LVTTTL, Slow, 8 mA	0.62	0.70	0.82	2.09	2.30	2.61	2.09	2.30	2.61	ns
LVTTTL, Slow, 12 mA	0.62	0.70	0.82	1.94	2.15	2.46	1.94	2.15	2.46	ns
LVTTTL, Slow, 16 mA	0.62	0.70	0.82	1.84	2.04	2.34	1.84	2.04	2.34	ns

**Table 30: IOB Switching Characteristics (Continued)**

I/O Standard	T <sub>IOPI</sub>			T <sub>IOOP</sub>			T <sub>IOTP</sub>			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2	-1	-3	-2	-1	-3	-2	-1	
LVTTTL, Slow, 24 mA	0.62	0.70	0.82	1.87	2.07	2.38	1.87	2.07	2.38	ns
LVTTTL, Fast, 2 mA	0.62	0.70	0.82	3.32	3.61	4.05	3.32	3.61	4.05	ns
LVTTTL, Fast, 4 mA	0.62	0.70	0.82	2.32	2.55	2.90	2.32	2.55	2.90	ns
LVTTTL, Fast, 6 mA	0.62	0.70	0.82	2.10	2.31	2.63	2.10	2.31	2.63	ns
LVTTTL, Fast, 8 mA	0.62	0.70	0.82	1.65	1.82	2.09	1.65	1.82	2.09	ns
LVTTTL, Fast, 12 mA	0.62	0.70	0.82	1.47	1.63	1.89	1.47	1.63	1.89	ns
LVTTTL, Fast, 16 mA	0.62	0.70	0.82	1.41	1.57	1.81	1.41	1.57	1.81	ns
LVTTTL, Fast, 24 mA	0.62	0.70	0.82	1.36	1.52	1.74	1.36	1.52	1.74	ns
LVC MOS33, Slow, 2 mA	0.62	0.70	0.82	3.63	3.96	4.44	3.63	3.96	4.44	ns
LVC MOS33, Slow, 4 mA	0.62	0.70	0.82	2.82	3.09	3.49	2.82	3.09	3.49	ns
LVC MOS33, Slow, 6 mA	0.62	0.70	0.82	2.61	2.86	3.24	2.61	2.86	3.24	ns
LVC MOS33, Slow, 8 mA	0.62	0.70	0.82	2.06	2.26	2.57	2.06	2.26	2.57	ns
LVC MOS33, Slow, 12 mA	0.62	0.70	0.82	1.95	2.14	2.42	1.95	2.14	2.42	ns
LVC MOS33, Slow, 16 mA	0.62	0.70	0.82	1.86	2.04	2.31	1.86	2.04	2.31	ns
LVC MOS33, Slow, 24 mA	0.62	0.70	0.82	1.87	2.07	2.35	1.87	2.07	2.35	ns
LVC MOS33, Fast, 2 mA	0.62	0.70	0.82	2.94	3.20	3.59	2.94	3.20	3.59	ns
LVC MOS33, Fast, 4 mA	0.62	0.70	0.82	2.27	2.50	2.84	2.27	2.50	2.84	ns
LVC MOS33, Fast, 6 mA	0.62	0.70	0.82	2.06	2.27	2.59	2.06	2.27	2.59	ns
LVC MOS33, Fast, 8 mA	0.62	0.70	0.82	1.61	1.79	2.05	1.61	1.79	2.05	ns
LVC MOS33, Fast, 12 mA	0.62	0.70	0.82	1.45	1.61	1.86	1.45	1.61	1.86	ns
LVC MOS33, Fast, 16 mA	0.62	0.70	0.82	1.40	1.56	1.80	1.40	1.56	1.80	ns
LVC MOS33, Fast, 24 mA	0.62	0.70	0.82	1.35	1.51	1.74	1.35	1.51	1.74	ns
LVC MOS25, Slow, 2 mA	0.61	0.70	0.82	3.67	3.97	4.42	3.67	3.97	4.42	ns
LVC MOS25, Slow, 4 mA	0.61	0.70	0.82	2.37	2.60	2.94	2.37	2.60	2.94	ns
LVC MOS25, Slow, 6 mA	0.61	0.70	0.82	2.19	2.41	2.74	2.19	2.41	2.74	ns
LVC MOS25, Slow, 8 mA	0.61	0.70	0.82	2.05	2.26	2.56	2.05	2.26	2.56	ns
LVC MOS25, Slow, 12 mA	0.61	0.70	0.82	2.10	2.31	2.63	2.10	2.31	2.63	ns
LVC MOS25, Slow, 16 mA	0.61	0.70	0.82	1.84	2.02	2.30	1.84	2.02	2.30	ns
LVC MOS25, Slow, 24 mA	0.61	0.70	0.82	1.83	2.04	2.34	1.83	2.04	2.34	ns
LVC MOS25, Fast, 2 mA	0.61	0.70	0.82	3.14	3.41	3.82	3.14	3.41	3.82	ns
LVC MOS25, Fast, 4 mA	0.61	0.70	0.82	1.89	2.08	2.37	1.89	2.08	2.37	ns
LVC MOS25, Fast, 6 mA	0.61	0.70	0.82	1.74	1.92	2.20	1.74	1.92	2.20	ns
LVC MOS25, Fast, 8 mA	0.61	0.70	0.82	1.66	1.83	2.09	1.66	1.83	2.09	ns
LVC MOS25, Fast, 12 mA	0.61	0.70	0.82	1.52	1.69	1.94	1.52	1.69	1.94	ns
LVC MOS25, Fast, 16 mA	0.61	0.70	0.82	1.43	1.60	1.85	1.43	1.60	1.85	ns
LVC MOS25, Fast, 24 mA	0.61	0.70	0.82	1.40	1.54	1.76	1.40	1.54	1.76	ns



**Table 30: IOB Switching Characteristics (Continued)**

I/O Standard	T <sub>IOPI</sub>			T <sub>IOOP</sub>			T <sub>IOTP</sub>			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2	-1	-3	-2	-1	-3	-2	-1	
LVC MOS18, Slow, 2 mA	0.67	0.76	0.89	4.20	4.56	5.09	4.20	4.56	5.09	ns
LVC MOS18, Slow, 4 mA	0.67	0.76	0.89	3.03	3.32	3.75	3.03	3.32	3.75	ns
LVC MOS18, Slow, 6 mA	0.67	0.76	0.89	2.37	2.61	2.97	2.37	2.61	2.97	ns
LVC MOS18, Slow, 8 mA	0.67	0.76	0.89	2.15	2.37	2.69	2.15	2.37	2.69	ns
LVC MOS18, Slow, 12 mA	0.67	0.76	0.89	1.95	2.16	2.47	1.95	2.16	2.47	ns
LVC MOS18, Slow, 16 mA	0.67	0.76	0.89	1.93	2.14	2.45	1.93	2.14	2.45	ns
LVC MOS18, Fast, 2 mA	0.67	0.76	0.89	3.41	3.71	4.16	3.41	3.71	4.16	ns
LVC MOS18, Fast, 4 mA	0.67	0.76	0.89	2.36	2.61	2.98	2.36	2.61	2.98	ns
LVC MOS18, Fast, 6 mA	0.67	0.76	0.89	1.87	2.06	2.35	1.87	2.06	2.35	ns
LVC MOS18, Fast, 8 mA	0.67	0.76	0.89	1.69	1.87	2.13	1.69	1.87	2.13	ns
LVC MOS18, Fast, 12 mA	0.67	0.76	0.89	1.51	1.68	1.93	1.51	1.68	1.93	ns
LVC MOS18, Fast, 16 mA	0.67	0.76	0.89	1.44	1.61	1.86	1.44	1.61	1.86	ns
LVC MOS15, Slow, 2 mA	0.73	0.83	0.98	3.50	3.84	4.34	3.50	3.84	4.34	ns
LVC MOS15, Slow, 4 mA	0.73	0.83	0.98	2.17	2.40	2.74	2.17	2.40	2.74	ns
LVC MOS15, Slow, 6 mA	0.73	0.83	0.98	1.99	2.20	2.52	1.99	2.20	2.52	ns
LVC MOS15, Slow, 8 mA	0.73	0.83	0.98	1.91	2.12	2.43	1.91	2.12	2.43	ns
LVC MOS15, Slow, 12 mA	0.73	0.83	0.98	1.74	1.95	2.25	1.74	1.95	2.25	ns
LVC MOS15, Slow, 16 mA	0.73	0.83	0.98	1.71	1.91	2.20	1.71	1.91	2.20	ns
LVC MOS15, Fast, 2 mA	0.73	0.83	0.98	2.80	3.07	3.48	2.80	3.07	3.48	ns
LVC MOS15, Fast, 4 mA	0.73	0.83	0.98	1.76	1.95	2.23	1.76	1.95	2.23	ns
LVC MOS15, Fast, 6 mA	0.73	0.83	0.98	1.62	1.80	2.06	1.62	1.80	2.06	ns
LVC MOS15, Fast, 8 mA	0.73	0.83	0.98	1.57	1.74	2.00	1.57	1.74	2.00	ns
LVC MOS15, Fast, 12 mA	0.73	0.83	0.98	1.43	1.60	1.86	1.43	1.60	1.86	ns
LVC MOS15, Fast, 16 mA	0.73	0.83	0.98	1.37	1.53	1.77	1.37	1.53	1.77	ns
LVC MOS12, Slow, 2 mA	0.84	0.96	1.14	3.58	3.98	4.58	3.58	3.98	4.58	ns
LVC MOS12, Slow, 4 mA	0.84	0.96	1.14	2.10	2.33	2.66	2.10	2.33	2.66	ns
LVC MOS12, Slow, 6 mA	0.84	0.96	1.14	2.00	2.18	2.45	2.00	2.18	2.45	ns
LVC MOS12, Slow, 8 mA	0.84	0.96	1.14	1.91	2.14	2.48	1.91	2.14	2.48	ns
LVC MOS12, Fast, 2 mA	0.84	0.96	1.14	3.05	3.38	3.87	3.05	3.38	3.87	ns
LVC MOS12, Fast, 4 mA	0.84	0.96	1.14	1.71	1.91	2.20	1.71	1.91	2.20	ns
LVC MOS12, Fast, 6 mA	0.84	0.96	1.14	1.58	1.78	2.08	1.58	1.78	2.08	ns
LVC MOS12, Fast, 8 mA	0.84	0.96	1.14	1.52	1.70	1.97	1.52	1.70	1.97	ns

**Table 30: IOB Switching Characteristics (Continued)**

I/O Standard	T <sub>IOPI</sub>			T <sub>IOOP</sub>			T <sub>IOTP</sub>			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2	-1	-3	-2	-1	-3	-2	-1	
LVDCI_33	0.62	0.70	0.82	1.50	1.66	1.90	1.50	1.66	1.90	ns
LVDCI_25	0.61	0.70	0.82	1.55	1.71	1.93	1.55	1.71	1.93	ns
LVDCI_18	0.67	0.76	0.89	1.65	1.78	1.99	1.65	1.78	1.99	ns
LVDCI_15	0.73	0.83	0.98	1.58	1.75	2.02	1.58	1.75	2.02	ns
LVDCI_DV2_25	0.61	0.70	0.82	1.36	1.51	1.74	1.36	1.51	1.74	ns
LVDCI_DV2_18	0.67	0.76	0.89	1.43	1.60	1.85	1.43	1.60	1.85	ns
LVDCI_DV2_15	0.73	0.83	0.98	1.48	1.65	1.91	1.48	1.65	1.91	ns
GTL_DCI	0.76	0.85	1.00	1.36	1.47	1.65	1.36	1.47	1.65	ns
GTLP_DCI	0.76	0.85	1.00	1.37	1.52	1.76	1.37	1.52	1.76	ns
LVPECL_25	0.80	0.90	1.06	1.28	1.42	1.62	1.28	1.42	1.62	ns
HSTL_I_12	0.76	0.85	1.00	1.45	1.61	1.85	1.45	1.61	1.85	ns
HSTL_I_DCI	0.76	0.85	1.00	1.41	1.56	1.77	1.41	1.56	1.77	ns
HSTL_II_DCI	0.76	0.85	1.00	1.34	1.48	1.69	1.34	1.48	1.69	ns
HSTL_II_T_DCI	0.76	0.85	1.00	1.41	1.56	1.77	1.41	1.56	1.77	ns
HSTL_III_DCI	0.76	0.85	1.00	1.57	1.72	1.95	1.57	1.72	1.95	ns
HSTL_IV_DCI	0.76	0.85	1.00	1.34	1.46	1.64	1.34	1.46	1.64	ns
HSTL_I_DCI_18	0.76	0.85	1.00	1.36	1.50	1.70	1.36	1.50	1.70	ns
HSTL_II_DCI_18	0.76	0.85	1.00	1.30	1.43	1.64	1.30	1.43	1.64	ns
HSTL_II_T_DCI_18	0.76	0.85	1.00	1.36	1.50	1.70	1.36	1.50	1.70	ns
HSTL_III_DCI_18	0.76	0.85	1.00	1.55	1.69	1.91	1.55	1.69	1.91	ns
HSTL_IV_DCI_18	0.76	0.85	1.00	1.31	1.44	1.62	1.31	1.44	1.62	ns
DIFF_HSTL_I_18	0.80	0.90	1.06	1.40	1.55	1.77	1.40	1.55	1.77	ns
DIFF_HSTL_I_DCI_18	0.80	0.90	1.06	1.36	1.50	1.70	1.36	1.50	1.70	ns
DIFF_HSTL_I	0.80	0.90	1.06	1.42	1.57	1.79	1.42	1.57	1.79	ns
DIFF_HSTL_I_DCI	0.80	0.90	1.06	1.41	1.56	1.77	1.41	1.56	1.77	ns
DIFF_HSTL_II_18	0.80	0.90	1.06	1.36	1.51	1.72	1.36	1.51	1.72	ns
DIFF_HSTL_II_DCI_18	0.80	0.90	1.06	1.30	1.43	1.64	1.30	1.43	1.64	ns
DIFF_HSTL_II	0.80	0.90	1.06	1.39	1.53	1.74	1.39	1.53	1.74	ns
DIFF_HSTL_II_DCI	0.80	0.90	1.06	1.34	1.48	1.69	1.34	1.48	1.69	ns

**Table 30: IOB Switching Characteristics (Continued)**

I/O Standard	$T_{IOPI}$			$T_{IOOP}$			$T_{IOTP}$			Units
	Speed Grade			Speed Grade			Speed Grade			
	-3	-2	-1	-3	-2	-1	-3	-2	-1	
SSTL2_I_DCI	0.76	0.85	1.00	1.42	1.56	1.78	1.42	1.56	1.78	ns
SSTL2_II_DCI	0.76	0.85	1.00	1.34	1.48	1.70	1.34	1.48	1.70	ns
SSTL2_II_T_DCI	0.76	0.85	1.00	1.42	1.56	1.78	1.42	1.56	1.78	ns
SSTL18_I	0.76	0.85	1.00	1.46	1.61	1.84	1.46	1.61	1.84	ns
SSTL18_II	0.76	0.85	1.00	1.39	1.53	1.75	1.39	1.53	1.75	ns
SSTL18_I_DCI	0.76	0.85	1.00	1.39	1.53	1.74	1.39	1.53	1.74	ns
SSTL18_II_DCI	0.76	0.85	1.00	1.30	1.44	1.64	1.30	1.44	1.64	ns
SSTL18_II_T_DCI	0.76	0.85	1.00	1.39	1.53	1.74	1.39	1.53	1.74	ns
DIFF_SSTL2_I	0.80	0.90	1.06	1.48	1.64	1.87	1.48	1.64	1.87	ns
DIFF_SSTL2_I_DCI	0.80	0.90	1.06	1.42	1.56	1.78	1.42	1.56	1.78	ns
DIFF_SSTL18_I	0.80	0.90	1.06	1.46	1.61	1.84	1.46	1.61	1.84	ns
DIFF_SSTL18_I_DCI	0.80	0.90	1.06	1.39	1.53	1.74	1.39	1.53	1.74	ns
DIFF_SSTL2_II	0.80	0.90	1.06	1.40	1.55	1.76	1.40	1.55	1.76	ns
DIFF_SSTL2_II_DCI	0.80	0.90	1.06	1.34	1.48	1.70	1.34	1.48	1.70	ns
DIFF_SSTL18_II	0.80	0.90	1.06	1.39	1.53	1.75	1.39	1.53	1.75	ns
DIFF_SSTL18_II_DCI	0.80	0.90	1.06	1.30	1.44	1.64	1.30	1.44	1.64	ns

**Table 31: IOB 3-state ON Output Switching Characteristics ( $T_{IOTPHZ}$ )**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$T_{IOTPHZ}$	T input to Pad high-impedance	0.88	1.01	1.12	ns

## I/O Standard Adjustment Measurement Methodology

### Input Delay Measurements

Table 32 shows the test setup parameters used for measuring input delay.

Table 32: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1,2)}$	$V_H^{(1,2)}$	$V_{MEAS}^{(1,4,5)}$	$V_{REF}^{(1,3,5)}$
LVTTTL (Low-Voltage Transistor-Transistor Logic)	LVTTTL	0	3.0	1.4	–
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	0	3.3	1.65	–
LVC MOS, 2.5V	LVC MOS25	0	2.5	1.25	–
LVC MOS, 1.8V	LVC MOS18	0	1.8	0.9	–
LVC MOS, 1.5V	LVC MOS15	0	1.5	0.75	–
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3	Per PCI Specification			–
PCI, 66 MHz, 3.3V	PCI66_3	Per PCI Specification			–
PCI-X, 133 MHz, 3.3V	PCIX	Per PCI-X Specification			–
GTL (Gunning Transceiver Logic)	GTL	$V_{REF} - 0.2$	$V_{REF} + 0.2$	$V_{REF}$	0.80
GTL Plus	GTL P	$V_{REF} - 0.2$	$V_{REF} + 0.2$	$V_{REF}$	1.0
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	$V_{REF}$	0.75
HSTL, Class III & IV	HSTL_III, HSTL_IV	$V_{REF} - 0.5$	$V_{REF} + 0.5$	$V_{REF}$	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	$V_{REF}$	0.90
HSTL, Class III & IV, 1.8V	HSTL_III_18, HSTL_IV_18	$V_{REF} - 0.5$	$V_{REF} + 0.5$	$V_{REF}$	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	$V_{REF} - 1.00$	$V_{REF} + 1.00$	$V_{REF}$	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	$V_{REF}$	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.5$	$V_{REF} + 0.5$	$V_{REF}$	0.90
AGP-2X/AGP (Accelerated Graphics Port)	AGP	$V_{REF} - (0.2 \times V_{CCO})$	$V_{REF} + (0.2 \times V_{CCO})$	$V_{REF}$	AGP Spec
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	$1.2 - 0.125$	$1.2 + 0.125$	1.2	
LVDS EXT (LVDS Extended Mode), 2.5V	LVDS EXT_25	$1.2 - 0.125$	$1.2 + 0.125$	1.2	
LDT (HyperTransport), 2.5V	LDT_25	$0.6 - 0.125$	$0.6 + 0.125$	0.6	
LVPECL (Low-Voltage Positive Electron-Coupled Logic), 2.5V	LVPECL_25	$1.15 - 0.3$	$1.15 - 0.3$	1.15	

#### Notes:

- Input delay measurement methodology parameters for LVDCI and HSLVDCI are the same as for LVC MOS standards of the same voltage. Parameters for all other DCI standards are the same as for the corresponding non-DCI standards.
- Input waveform switches between  $V_L$  and  $V_H$ .
- Measurements are made at typical, minimum, and maximum  $V_{REF}$  values. Reported delays reflect worst case of these measurements.  $V_{REF}$  values listed are typical.
- Input voltage level from which measurement starts.
- This is an input voltage reference that bears no relation to the  $V_{REF} / V_{MEAS}$  parameters found in IBIS models and/or noted in Figure 6.

### Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setup shown in **Figure 6**.

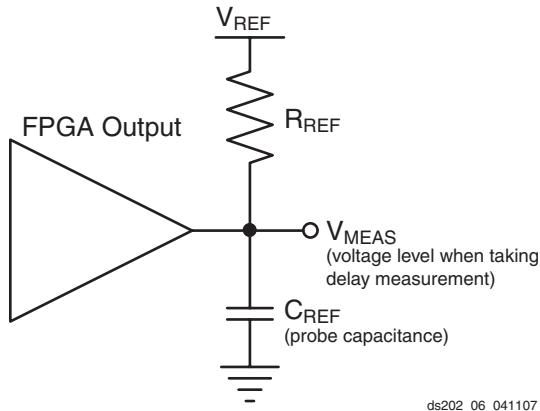


Figure 6: Generalized Test Setup

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters  $V_{REF}$ ,  $R_{REF}$ ,  $C_{REF}$ , and  $V_{MEAS}$  fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from **Table 33**.
2. Record the time to  $V_{MEAS}$ .
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to  $V_{MEAS}$ .
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual worst-case propagation delay (clock-to-input) of the PCB trace.

Table 33: Output Delay Measurement Methodology

Description	I/O Standard Attribute	$R_{REF}$ ( $\Omega$ )	$C_{REF}^{(1)}$ (pF)	$V_{MEAS}$ (V)	$V_{REF}$ (V)
LVTTTL (Low-Voltage Transistor-Transistor Logic)	LVTTTL (all)	1M	0	1.4	0
LVC MOS (Low-Voltage CMOS), 3.3V	LVC MOS33	1M	0	1.65	0
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.2V	LVC MOS12	1M	0	0.75	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	10 <sup>(2)</sup>	0.94	0
	PCI33_3 (falling edge)	25	10 <sup>(2)</sup>	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	10 <sup>(2)</sup>	0.94	0
	PCI66_3 (falling edge)	25	10 <sup>(2)</sup>	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	10 <sup>(3)</sup>	0.94	
	PCIX (falling edge)	25	10 <sup>(3)</sup>	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	$V_{REF}$	0.75
HSTL, Class II	HSTL_II	25	0	$V_{REF}$	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	$V_{REF}$	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	$V_{REF}$	0.9

Table 33: Output Delay Measurement Methodology (Continued)

Description	I/O Standard Attribute	R <sub>REF</sub> (Ω)	C <sub>REF</sub> <sup>(1)</sup> (pF)	V <sub>MEAS</sub> (V)	V <sub>REF</sub> (V)
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V <sub>REF</sub>	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V <sub>REF</sub>	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V <sub>REF</sub>	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V <sub>REF</sub>	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	50	0	V <sub>REF</sub>	1.2
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	50	0	V <sub>REF</sub>	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	1M	0	1.2	0
LDT (HyperTransport), 2.5V	LDT_25	50	0	V <sub>REF</sub>	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	1M	0	0.90	0
LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33, HSLVDCI_33	1M	0	1.65	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V <sub>REF</sub>	0.75
HSTL, Class III & IV, with DCI	HSTL_III_DCI, HSTL_IV_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V <sub>REF</sub>	0.9
HSTL, Class III & IV, 1.8V, with DCI	HSTL_III_DCI_18, HSTL_IV_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termini.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V <sub>REF</sub>	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V <sub>REF</sub>	1.25
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	50	0	0.8	1.2
GTL Plus with DCI	GTLP_DCI	50	0	1.0	1.5

**Notes:**

- C<sub>REF</sub> is the capacitance of the probe, nominally 0 pF.
- Per PCI specifications.
- Per PCI-X specifications.

## Input/Output Logic Switching Characteristics

Table 34: ILOGIC Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Setup/Hold</b>					
$T_{ICE1CK}/T_{ICKCE1}$	CE1 pin Setup/Hold with respect to CLK	0.43 -0.24	0.49 -0.24	0.59 -0.24	ns
$T_{ISRCK}/T_{ICKSR}$	SR/REV pin Setup/Hold with respect to CLK	0.85 -0.20	1.00 -0.20	1.22 -0.20	ns
$T_{IDOCK}/T_{IOCKD}$	D pin Setup/Hold with respect to CLK without Delay	0.34 -0.12	0.37 -0.12	0.39 -0.12	ns
$T_{IDOCKD}/T_{IOCKDD}$	DDL Y pin Setup/Hold with respect to CLK (using IODELAY)	0.31 -0.09	0.33 -0.09	0.36 -0.08	ns
<b>Combinatorial</b>					
$T_{IDI}$	D pin to O pin propagation delay, no Delay	0.24	0.26	0.30	ns
$T_{IDID}$	DDL Y pin to O pin propagation delay (using IODELAY)	0.20	0.22	0.26	ns
<b>Sequential Delays</b>					
$T_{IDLO}$	D pin to Q1 pin using flip-flop as a latch without Delay	0.44	0.50	0.58	ns
$T_{IDL0D}$	DDL Y pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.41	0.46	0.55	ns
$T_{ICKQ}$	CLK to Q outputs	0.47	0.52	0.60	ns
$T_{RQ}$	SR/REV pin to OQ/TQ out	1.12	1.28	1.53	ns
$T_{GSRQ}$	Global Set/Reset to Q outputs	7.30	7.30	10.10	ns
<b>Set/Reset</b>					
$T_{RPW}$	Minimum Pulse Width, SR/REV inputs	0.78	0.95	1.20	ns, Min

Table 35: OLOGIC Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Setup/Hold</b>					
$T_{ODCK}/T_{OCKD}$	D1/D2 pins Setup/Hold with respect to CLK	0.30 -0.21	0.36 -0.21	0.44 -0.21	ns
$T_{OOCECK}/T_{OCKOCE}$	OCE pin Setup/Hold with respect to CLK	0.16 -0.07	0.19 -0.07	0.23 -0.07	ns
$T_{OSRCK}/T_{OCKSR}$	SR/REV pin Setup/Hold with respect to CLK	0.93 -0.20	1.02 -0.20	1.16 -0.20	ns
$T_{OTCK}/T_{OCKT}$	T1/T2 pins Setup/Hold with respect to CLK	0.28 -0.18	0.34 -0.18	0.41 -0.18	ns
$T_{OTCECK}/T_{OCKTCE}$	TCE pin Setup/Hold with respect to CLK	0.20 -0.06	0.23 -0.06	0.29 -0.06	ns
<b>Combinatorial</b>					
$T_{DOQ}$	D1 to OQ out or T1 to TQ out	0.62	0.70	0.83	ns
<b>Sequential Delays</b>					
$T_{OCKQ}$	CLK to OQ/TQ out	0.61	0.62	0.62	ns
$T_{RQ}$	SR/REV pin to OQ/TQ out	1.63	1.89	2.27	ns
$T_{GSRQ}$	Global Set/Reset to Q outputs	7.30	7.30	10.10	ns
<b>Set/Reset</b>					
$T_{RPW}$	Minimum Pulse Width, SR/REV inputs	0.80	0.98	1.25	ns, Min



## Input Serializer/Deserializer Switching Characteristics

Table 36: ISERDES Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Setup/Hold for Control Lines</b>					
$T_{ISCK\_BITSLIP} / T_{ISCK\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.10 0.00	0.11 0.00	0.12 0.00	ns
$T_{ISCK\_CE} / T_{ISCK\_CE}^{(2)}$	CE pin Setup/Hold with respect to CLK (for CE1)	0.43 -0.24	0.49 -0.24	0.59 -0.24	ns
$T_{ISCK\_CE2} / T_{ISCK\_CE2}^{(2)}$	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.03 0.11	0.04 0.13	0.06 0.15	ns
<b>Setup/Hold for Data Lines</b>					
$T_{ISDCK\_D} / T_{ISCKD\_D}$	D pin Setup/Hold with respect to CLK	0.34 -0.12	0.37 -0.12	0.39 -0.12	ns
$T_{ISDCK\_DDL} / T_{ISCKD\_DDL}$	DDL pin Setup/Hold with respect to CLK (using IODELAY)	0.31 -0.09	0.33 -0.09	0.36 -0.08	ns
$T_{ISDCK\_DDR} / T_{ISCKD\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	0.34 -0.12	0.37 -0.12	0.39 -0.12	ns
$T_{ISDCK\_DDL\_DDR} / T_{ISCKD\_DDL\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY)	0.31 -0.09	0.33 -0.09	0.36 -0.08	ns
<b>Sequential Delays</b>					
$T_{ISCKO\_Q}$	CLKDIV to out at Q pin	0.46	0.51	0.60	ns
<b>Propagation Delays</b>					
$T_{ISDO\_DO}$	D input to DO output pin	0.20	0.22	0.26	ns

**Notes:**

- Recorded at 0 tap value.
- $T_{ISCK\_CE2}$  and  $T_{ISCK\_CE2}^{(2)}$  are reported as  $T_{ISCK\_CE} / T_{ISCK\_CE}$  in TRACE report.

## Output Serializer/Deserializer Switching Characteristics Input Delay Switching Characteristics

Table 37: OSERDES Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Setup/Hold</b>					
$T_{OSDCK\_D}/T_{OSCKD\_D}$	D input Setup/Hold with respect to CLKDIV	0.21 -0.02	0.24 -0.02	0.30 -0.02	ns
$T_{OSDCK\_T}/T_{OSCKD\_T}^{(1)}$	T input Setup/Hold with respect to CLK	0.28 -0.18	0.34 -0.18	0.41 -0.18	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}^{(1)}$	T input Setup/Hold with respect to CLKDIV	0.21 -0.03	0.24 -0.03	0.28 -0.03	ns
$T_{OSCK\_OCE}/T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK	0.16 -0.07	0.19 -0.07	0.23 -0.07	ns
$T_{OSCK\_S}$	SR (Reset) input Setup with respect to CLKDIV	0.52	0.58	0.70	ns
$T_{OSCK\_TCE}/T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK	0.20 -0.06	0.23 -0.06	0.29 -0.06	ns
<b>Sequential Delays</b>					
$T_{OSCKO\_OQ}$	Clock to out from CLK to OQ	0.59	0.60	0.61	ns
$T_{OSCKO\_TQ}$	Clock to out from CLK to TQ	0.61	0.62	0.62	ns
<b>Combinatorial</b>					
$T_{OSDO\_TQ}$	T input to TQ Out	0.62	0.70	0.83	ns
$T_{OSCO\_OQ}$	Asynchronous Reset to OQ	1.57	1.82	2.19	ns
$T_{OSCO\_TQ}$	Asynchronous Reset to TQ	1.63	1.89	2.27	ns

**Notes:**

- $T_{OSDCK\_T2}$  and  $T_{OSCKD\_T2}$  are reported as  $T_{OSDCK\_T}/T_{OSCKD\_T}$  in TRACE report.

**Table 38: Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
T <sub>IDELAYRESOLUTION</sub>	IODELAY Chain Delay Resolution	1/(64 x F <sub>REF</sub> x 1e <sup>6</sup> ) <sup>(1)</sup>			ps
T <sub>IDELAYCTRLCO_RDY</sub>	Reset to Ready for IDELAYCTRL	3.00	3.00	3.00	µs
F <sub>IDELAYCTRL_REF</sub>	REFCLK frequency	200.00	200.00	200.00	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
T <sub>IDELAYCTRL_RPW</sub>	Minimum Reset pulse width	50.00	50.00	50.00	ns
T <sub>IDELAYPAT_JIT</sub>	Pattern dependent period jitter in delay chain for clock pattern	0	0	0	Note 2
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)	±5	±5	±5	Note 2
T <sub>IODELAY_CLK_MAX</sub>	Maximum frequency of CLK input to IODELAY	300	250	250	MHz
T <sub>IODCK_CE</sub> / T <sub>IODCKC_CE</sub>	CE pin Setup/Hold with respect to CK	0.29 -0.06	0.34 -0.06	0.42 -0.06	ns
T <sub>IODCK_INC</sub> / T <sub>IODCKC_INC</sub>	INC pin Setup/Hold with respect to CK	0.18 0.02	0.20 0.04	0.24 0.06	ns
T <sub>IODCK_RST</sub> / T <sub>IODCKC_RST</sub>	RST pin Setup/Hold with respect to CK	0.25 -0.12	0.28 -0.12	0.33 -0.12	ns

**Notes:**

1. Average Tap Delay at 200 MHz = 78 ps.
2. Units in ps, peak-to-peak per tap, in High Performance mode.

## CLB Switching Characteristics

**Table 39: CLB Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Combinatorial Delays</b>					
T <sub>ILO</sub>	An – Dn LUT address to A	0.08	0.09	0.10	ns, Max
	An – Dn LUT address to AMUX/CMUX	0.20	0.22	0.25	ns, Max
	An – Dn LUT address to BMUX_A	0.31	0.35	0.40	ns, Max
T <sub>ITO</sub>	An – Dn inputs to A – D Q outputs	0.67	0.77	0.90	ns, Max
T <sub>AXA</sub>	AX inputs to AMUX output	0.39	0.44	0.53	ns, Max
T <sub>AXB</sub>	AX inputs to BMUX output	0.46	0.52	0.61	ns, Max
T <sub>AXC</sub>	AX inputs to CMUX output	0.31	0.36	0.42	ns, Max
T <sub>AXD</sub>	AX inputs to DMUX output	0.55	0.62	0.73	ns, Max
T <sub>BXB</sub>	BX inputs to BMUX output	0.36	0.41	0.48	ns, Max
T <sub>BXD</sub>	BX inputs to DMUX output	0.45	0.51	0.59	ns, Max
T <sub>CXB</sub>	CX inputs to CMUX output	0.33	0.36	0.42	ns, Max
T <sub>CXD</sub>	CX inputs to DMUX output	0.37	0.42	0.49	ns, Max
T <sub>DXD</sub>	DX inputs to DMUX output	0.38	0.42	0.49	ns, Max

**Table 39: CLB Switching Characteristics (Continued)**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
T <sub>OPCYA</sub>	An input to COUT output	0.43	0.50	0.59	ns, Max
T <sub>OPCYB</sub>	Bn input to COUT output	0.39	0.44	0.51	ns, Max
T <sub>OPCYC</sub>	Cn input to COUT output	0.33	0.37	0.43	ns, Max
T <sub>OPCYD</sub>	Dn input to COUT output	0.30	0.34	0.40	ns, Max
T <sub>AXCY</sub>	AX input to COUT output	0.36	0.42	0.50	ns, Max
T <sub>BXCY</sub>	BX input to COUT output	0.26	0.30	0.37	ns, Max
T <sub>CXCY</sub>	CX input to COUT output	0.20	0.22	0.26	ns, Max
T <sub>DXCY</sub>	DX input to COUT output	0.20	0.22	0.26	ns, Max
T <sub>BYP</sub>	CIN input to COUT output	0.09	0.10	0.11	ns, Max
T <sub>CINA</sub>	CIN input to AMUX output	0.24	0.27	0.31	ns, Max
T <sub>CINB</sub>	CIN input to BMUX output	0.27	0.30	0.35	ns, Max
T <sub>CINC</sub>	CIN input to CMUX output	0.29	0.32	0.36	ns, Max
T <sub>CIND</sub>	CIN input to DMUX output	0.31	0.35	0.41	ns, Max
<b>Sequential Delays</b>					
T <sub>CKO</sub>	Clock to AQ – DQ outputs	0.35	0.40	0.47	ns, Max
<b>Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK</b>					
T <sub>DICK</sub> /T <sub>CKDI</sub>	A – D input to CLK on A – D Flip Flops	0.36 0.19	0.41 0.21	0.49 0.24	ns, Min
T <sub>RCK</sub>	DX input to CLK when used as REV	0.37	0.42	0.51	ns, Min
T <sub>CECK</sub> /T <sub>CKCE</sub>	CE input to CLK on A – D Flip Flops	0.18 –0.04	0.20 –0.04	0.23 –0.04	ns, Min
T <sub>SRCK</sub> /T <sub>CKSR</sub>	SR input to CLK on A – D Flip Flops	0.41 –0.19	0.49 –0.19	0.59 –0.19	ns, Min
T <sub>CINCK</sub> /T <sub>CKCIN</sub>	CIN input to CLK on A – D Flip Flops	0.14 0.14	0.16 0.16	0.18 0.19	ns, Min
<b>Set/Reset</b>					
T <sub>SRMIN</sub>	SR input minimum pulse width	0.90	0.90	0.90	ns, Min
T <sub>RQ</sub>	Delay from SR or REV input to AQ – DQ flip-flops	0.74	0.86	1.03	ns, Max
T <sub>CEO</sub>	Delay from CE input to AQ – DQ flip-flops	0.46	0.52	0.63	ns, Max
F <sub>TOG</sub>	Toggle frequency (for export control)	1412	1265	1098	MHz

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

## CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 40: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Sequential Delays</b>					
$T_{SHCKO}$	Clock to A – B outputs	1.08	1.26	1.54	ns, Max
$T_{SHCKO\_1}$	Clock to AMUX – BMUX outputs	1.19	1.38	1.68	ns, Max
<b>Setup and Hold Times Before/After Clock CLK</b>					
$T_{DS}/T_{DH}$	A – D inputs to CLK	0.72 0.20	0.84 0.22	1.03 0.26	ns, Min
$T_{AS}/T_{AH}$	Address An inputs to clock	0.41 0.20	0.46 0.22	0.54 0.27	ns, Min
$T_{WS}/T_{WH}$	WE input to clock	0.34 -0.06	0.39 -0.04	0.46 -0.02	ns, Min
$T_{CECK}/T_{CKCE}$	CE input to CLK	0.36 -0.08	0.42 -0.07	0.51 -0.06	ns, Min
<b>Clock CLK</b>					
$T_{MPW}$	Minimum pulse width	0.70	0.82	1.00	ns, Min
$T_{MCP}$	Minimum clock period	1.40	1.64	2.00	ns, Min

**Notes:**

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2.  $T_{SHCKO}$  also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

## CLB Shift Register Switching Characteristics (SLICEM Only)

Table 41: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Sequential Delays</b>					
$T_{REG}$	Clock to A – D outputs	1.23	1.43	1.73	ns, Max
$T_{REG\_MUX}$	Clock to AMUX – DMUX output	1.33	1.55	1.87	ns, Max
$T_{REG\_M31}$	Clock to DMUX output via M31 output	0.99	1.15	1.38	ns, Max
<b>Setup and Hold Times Before/After Clock CLK</b>					
$T_{WS}/T_{WH}$	WE input	0.21 -0.06	0.24 -0.04	0.29 -0.02	ns, Min
$T_{CECK}/T_{CKCE}$	CE input to CLK	0.23 -0.08	0.27 -0.07	0.33 -0.06	ns, Min
$T_{DS}/T_{DH}$	A – D inputs to CLK	0.57 0.07	0.66 0.09	0.78 0.11	ns, Min

Table 41: CLB Shift Register Switching Characteristics (Continued)

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Clock CLK</b>					
T <sub>MPW</sub>	Minimum pulse width	0.60	0.70	0.85	ns, Min

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

## Block RAM and FIFO Switching Characteristics

Table 42: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Block RAM and FIFO Clock to Out Delays</b>					
T <sub>RCKO_DO</sub> and T <sub>RCKO_DOR</sub> <sup>(1)</sup>	Clock CLK to DOUT output (without output register) <sup>(2)(3)</sup>	1.79	1.92	2.19	ns, Max
	Clock CLK to DOUT output (with output register) <sup>(4)(5)</sup>	0.61	0.69	0.82	ns, Max
	Clock CLK to DOUT output with ECC (without output register) <sup>(2)(3)</sup>	2.64	3.03	3.61	ns, Max
	Clock CLK to DOUT output with ECC (with output register) <sup>(4)(5)</sup>	0.66	0.77	0.93	ns, Max
	Clock CLK to DOUT output with Cascade (without output register) <sup>(2)</sup>	2.10	2.44	2.94	ns, Max
	Clock CLK to DOUT output with Cascade (with output register) <sup>(4)</sup>	0.91	1.07	1.30	ns, Max
T <sub>RCKO_FLAGS</sub>	Clock CLK to FIFO flags outputs <sup>(6)</sup>	0.76	0.87	1.02	ns, Max
T <sub>RCKO_POINTERS</sub>	Clock CLK to FIFO pointer outputs <sup>(7)</sup>	1.10	1.26	1.48	ns, Max
T <sub>RCKO_ECCR</sub>	Clock CLK to BITERR (with output register)	0.66	0.77	0.93	ns, Max
T <sub>RCKO_ECC</sub>	Clock CLK to BITERR (without output register)	2.48	2.85	3.41	ns, Max
	Clock CLK to ECCPARITY in standard ECC mode	1.29	1.47	1.74	ns, Max
	Clock CLK to ECCPARITY in ECC encode only mode	0.77	0.89	1.05	ns, Max

**Table 42: Block RAM and FIFO Switching Characteristics (Continued)**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Setup and Hold Times Before/After Clock CLK</b>					
$T_{RCKC\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs	0.34 0.30	0.40 0.32	0.48 0.36	ns, Min
$T_{RDCK\_DI}/T_{RDCK\_DI}$	DIN inputs <sup>(8)</sup>	0.27 0.28	0.30 0.28	0.35 0.29	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RDCK\_DI\_ECC}$	DIN inputs with ECC in standard mode <sup>(8)</sup>	0.33 0.32	0.37 0.33	0.42 0.36	ns, Min
	DIN inputs with ECC encode only <sup>(8)</sup>	0.68 0.32	0.72 0.33	0.77 0.36	ns, Min
$T_{RCKC\_EN}/T_{RCKC\_EN}$	Block RAM Enable (EN) input	0.32 0.15	0.36 0.15	0.42 0.15	ns, Min
$T_{RCKC\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.15 0.22	0.16 0.24	0.18 0.27	ns, Min
$T_{RCKC\_SSR}/T_{RCKC\_SSR}$	Synchronous Set/ Reset (SSR) input	0.17 0.23	0.21 0.25	0.26 0.28	ns, Min
$T_{RCKC\_WE}/T_{RCKC\_WE}$	Write Enable (WE) input	0.44 0.16	0.51 0.17	0.63 0.18	ns, Min
$T_{RCKC\_WREN}/T_{RCKC\_WREN}$	WREN/RDEN FIFO inputs <sup>(9)</sup>	0.36 0.30	0.41 0.34	0.48 0.40	ns, Min
<b>Reset Delays</b>					
$T_{RCO\_FLAGS}$	Reset RST to FIFO Flags/Pointers <sup>(10)</sup>	1.10	1.26	1.48	ns, Max
<b>Maximum Frequency</b>					
$F_{MAX}$	Block RAM in all modes	550	500	450	MHz
$F_{MAX\_CASCADE}$	Block RAM in Cascade mode	500	450	400	MHz
$F_{MAX\_FIFO}$	FIFO in all modes	550	500	450	MHz
$F_{MAX\_ECC}$	Block RAM in ECC mode	415	375	325	MHz

**Notes:**

- Trace will report all of these parameters as  $T_{RCKO\_DO}$ .
- $T_{RCKO\_DOR}$  includes  $T_{RCKO\_DOW}$ ,  $T_{RCKO\_DOPR}$ , and  $T_{RCKO\_DOPW}$  as well as the B port equivalent timing parameters.
- These parameters also apply to synchronous FIFO with  $DO\_REG = 0$ .
- $T_{RCKO\_DO}$  includes  $T_{RCKO\_DOP}$  as well as the B port equivalent timing parameters.
- These parameters also apply to multirate (asynchronous) and synchronous FIFO with  $DO\_REG = 1$ .
- $T_{RCKO\_FLAGS}$  includes the following parameters:  $T_{RCKO\_AEMPTY}$ ,  $T_{RCKO\_AFULL}$ ,  $T_{RCKO\_EMPTY}$ ,  $T_{RCKO\_FULL}$ ,  $T_{RCKO\_RDERR}$ ,  $T_{RCKO\_WRERR}$ .
- $T_{RCKO\_POINTERS}$  includes both  $T_{RCKO\_RDCOUNT}$  and  $T_{RCKO\_WRCOUNT}$ .
- $T_{RCKO\_DI}$  includes both A and B inputs as well as the parity inputs of A and B.
- These parameters also apply to RDEN.
- $T_{RCO\_FLAGS}$  includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.

## DSP48E Switching Characteristics

Table 43: DSP48E Switching Characteristics

Symbol	Description	Speed			Units
		-3	-2	-1	
<b>Setup and Hold Times of Data/Control Pins to the Input Register Clock</b>					
TDSPDCK_{AA, BB, ACINA, BCINB}/ TDSPCKD_{AA, BB, ACINA, BCINB}	{A, B, ACIN, BCIN} input to {A, B} register CLK	0.17 0.17	0.21 0.23	0.26 0.30	ns
TDSPDCK_CC/TDSPCKD_CC	C input to C register CLK	0.14 0.26	0.16 0.31	0.20 0.37	ns
<b>Setup and Hold Times of Data Pins to the Pipeline Register Clock</b>					
TDSPDCK_{AM, BM, ACINM, BCINM}/ TDSPCKD_{AM, BM, ACINM, BCINM}	{A, B, ACIN, BCIN} input to M register CLK	1.30 0.19	1.44 0.19	1.71 0.19	ns
<b>Setup and Hold Times of Data/Control Pins to the Output Register Clock</b>					
TDSPDCK_{AP, BP, ACINP, BCINP}_M/ TDSPCKD_{AP, BP, ACINP, BCINP}_M	{A, B, ACIN, BCIN} input to P register CLK using multiplier	2.39 -0.30	2.74 -0.30	3.25 -0.30	ns
TDSPDCK_{AP, BP, ACINP, BCINP}_NM/ TDSPCKD_{AP, BP, ACINP, BCINP}_NM	{A, B, ACIN, BCIN} input to P register CLK not using multiplier	1.35 -0.10	1.54 -0.10	1.83 -0.10	ns
TDSPDCK_CP/TDSPCKD_CP	C input to P register CLK	1.30 -0.13	1.42 -0.13	1.70 -0.13	ns
TDSPDCK_{PCINP, CRYCINP, MULTSIGNINP}/ TDSPCKD_{PCINP, CRYCINP, MULTSIGNINP}	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.06 0.11	1.17 0.11	1.31 0.11	ns
<b>Setup and Hold Times of the CE Pins</b>					
TDSPCCK_{CEA1A, CEA2A, CEB1B, CEB2B}/ TDSPCKC_{CEA1A, CEA2A, CEB1A, CEB2B}	{CEA1, CEA2A, CEB1B, CEB2B} input to {A, B} register CLK	0.24 0.21	0.28 0.25	0.33 0.31	ns
TDSPCCK_CECC/TDSPCKC_CECC	CEC input to C register CLK	0.19 0.17	0.21 0.21	0.26 0.28	ns
TDSPCCK_CEMM/TDSPCKC_CEMM	CEM input to M register CLK	0.25 0.18	0.29 0.21	0.36 0.26	ns
TDSPCCK_CEPP/TDSPCKC_CEPP	CEP input to P register CLK	0.56 0.01	0.63 0.01	0.73 0.01	ns
<b>Setup and Hold Times of the RST Pins</b>					
TDSPCCK_{RSTAA, RSTBB}/ TDSPCKC_{RSTAA, RSTBB}	{RSTA, RSTB} input to {A, B} register CLK	0.24 0.23	0.28 0.26	0.33 0.31	ns
TDSPCCK_RSTCC/TDSPCKC_RSTCC	RSTC input to C register CLK	0.19 0.17	0.21 0.21	0.26 0.28	ns
TDSPCCK_RSTMM/TDSPCKC_RSTMM	RSTM input to M register CLK	0.25 0.18	0.29 0.21	0.36 0.26	ns
TDSPCCK_RSTPP/TDSPCKC_RSTPP	RSTP input to P register CLK	0.56 0.01	0.63 0.01	0.73 0.01	ns



**Table 43: DSP48E Switching Characteristics (Continued)**

Symbol	Description	Speed			Units
		-3	-2	-1	
<b>Combinatorial Delays from Input Pins to Output Pins</b>					
TDSPDO_{AP, ACRYOUT, BP, BCRYOUT}_M	{A, B} input to {P, CARRYOUT} output using multiplier	2.78	3.22	3.84	ns
TDSPDO_{AP, ACRYOUT, BP, BCRYOUT}_NM	{A, B} input to {P, CARRYOUT} output not using multiplier	1.59	1.77	2.22	ns
TDSPDO_{CP, CCRYOUT, CRYINP, CRYINCRYOUT}	{C, CARRYIN} input to {P, CARRYOUT} output	1.50	1.67	2.08	ns
<b>Combinatorial Delays from Input Pins to Cascading Output Pins</b>					
TDSPDO_{AACOUT, BBCOUT}	{A, B} input to {ACOUT, BCOUT} output	1.00	1.12	1.31	ns
TDSPDO_{APCOUT, ACRYCOUT, AMULTSIGNOUT, BPCOUT, BCRYCOUT, BMULTSIGNOUT}_M	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	2.78	3.22	3.84	ns
TDSPDO_{APCOUT, ACRYCOUT, AMULTSIGNOUT, BPCOUT, BCRYCOUT, BMULTSIGNOUT}_NM	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.72	1.92	2.42	ns
TDSPDO_{CPCOUT, CCRYCOUT, CMULTSIGNOUT, CRYINPCOUT, CRYINCRYCOUT, CRYINMULTSIGNOUT}	{C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.63	1.82	2.28	ns
<b>Combinatorial Delays from Cascading Input Pins to All Output Pins</b>					
TDSPDO_{ACINP, ACINCRYOUT, BCINP, BCINCRYOUT}_M	{ACIN, BCIN} input to {P, CARRYOUT} output using multiplier	2.78	3.22	3.84	ns
TDSPDO_{ACINP, ACINCRYOUT, BCINP, BCINCRYOUT}_NM	{ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier	1.59	1.77	2.22	ns
TDSPDO_{ACINACOUT, BCINBCOUT}	{ACIN, BCIN} input to {ACOUT, BCOUT} output	1.00	1.12	1.31	ns
TDSPDO_{ACINPCOUT, ACINCRYCOUT, ACINMULTSIGNOUT, BCINPCOUT, BCINCRYCOUT, BCINMULTSIGNOUT}_M	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	2.78	3.22	3.84	ns
TDSPDO_{ACINPCOUT, ACINCRYCOUT, ACINMULTSIGNOUT, BCINPCOUT, BCINCRYCOUT, BCINMULTSIGNOUT}_NM	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.72	1.92	2.42	ns
TDSPDO_{PCINP, CRYCINP, MULTSIGNINP, PCINCRYOUT, CRYCINCRYOUT, MULTSIGNINCRYOUT}	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output	1.30	1.45	1.82	ns
TDSPDO_{PCINPCOUT, CRYCINPCOUT, MULTSIGNINPCOUT, PCINCRYCOUT, CRYCINCRYCOUT, MULTSIGNINCRYCOUT, PCINMULTSIGNOUT, CRYCINMULTSIGNOUT, MULTSIGNINMULTSIGNOUT}	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.43	1.60	2.02	ns
<b>Clock to Outs from Output Register Clock to Output Pins</b>					
TDSPCKO_{PP, CRYOUTP}	CLK (PREG) to {P, CARRYOUT} output	0.45	0.48	0.56	ns
TDSPCKO_{CRYCOUTP, PCOUTP, MULTSIGNOUTP}	CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output	0.48	0.53	0.62	ns

Table 43: DSP48E Switching Characteristics (Continued)

Symbol	Description	Speed			Units
		-3	-2	-1	
<b>Clock to Outs from Pipeline Register Clock to Output Pins</b>					
TDSPCKO_{PM, CRYOUTM}	CLK (MREG) to {P, CARRYOUT} output	1.81	2.10	2.47	ns
TDSPCKO_{PCOUTM, CRYCOUTM, MULTSIGNOUTM}	CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.91	2.13	2.66	ns
<b>Clock to Outs from Input Register Clock to Output Pins</b>					
TDSPCKO_{PA, CRYOUTA, PB, CRYOUTB}_M	CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier	3.09	3.57	4.23	ns
TDSPCKO_{PA, CRYOUTA, PB, CRYOUTB}_NM	CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier	1.90	2.11	2.63	ns
TDSPCKO_{PC, CRYOUTC}	CLK (CREG) to {P, CARRYOUT} output	1.89	2.11	2.62	ns
<b>Clock to Outs from Input Register Clock to Cascading Output Pins</b>					
TDSPCKO_{ACOUTA, BCOUTB}	CLK (AREG, BREG) to {ACOUT, BCOUT}	0.61	0.68	0.79	ns
TDSPCKO_{PCOUTA, CRYCOUTA, MULTSIGNOUTA, PCOUTB, CRYCOUTB, MULTSIGNOUTB}_M	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.09	3.57	4.23	ns
TDSPCKO_{PCOUTA, CRYCOUTA, MULTSIGNOUTA, PCOUTB, CRYCOUTB, MULTSIGNOUTB}_NM	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.03	2.27	2.82	ns
TDSPCKO_{PCOUTC, CRYCOUTC, MULTSIGNOUTC}	CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.03	2.26	2.82	ns
<b>Maximum Frequency</b>					
F <sub>MAX</sub>	With all registers used	550	500	450	MHz
F <sub>MAX_PATDET</sub>	With pattern detector	515	465	410	MHz
F <sub>MAX_MULT_NOMREG</sub>	Two register multiply without MREG	374	324	275	MHz
F <sub>MAX_MULT_NOMREG_PATDET</sub>	Two register multiply without MREG with pattern detect	345	300	254	MHz

## Configuration Switching Characteristics

Table 44: Configuration Switching Characteristics

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Power-up Timing Characteristics</b>					
$T_{PL}$	Program Latency	3	3	3	ms, Max
$T_{POR}$	Power-on-Reset	10 50	10 50	10 50	ms, Min/Max
$T_{ICCK}$	CCLK (output) delay	400	400	400	ns, Min
$T_{PROGRAM}$	Program Pulse Width	250	250	250	ns, Min
<b>Master/Slave Serial Mode Programming Switching<sup>(1)</sup></b>					
$T_{DCCK}/T_{CCKD}$	DIN Setup/Hold, slave mode	4.0 0.0	4.0 0.0	4.0 0.0	ns, Min
$T_{DSCCK}/T_{SCCKD}$	DIN Setup/Hold, master mode	4.0 0.0	4.0 0.0	4.0 0.0	ns, Min
$T_{CCO}$	DOUT	7.5	7.5	7.5	ns, Max
$F_{MCCK}$	Maximum Frequency, master mode with respect to nominal CCLK.	100	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode with respect to nominal CCLK.	±50	±50	±50	%
$F_{MSCCK}$	Slave mode external CCLK	100	100	100	MHz
<b>SelectMAP Mode Programming Switching<sup>(1)</sup></b>					
$T_{SMDCK}/T_{SMCKD}$	SelectMAP Data Setup/Hold	3.0 0.5	3.0 0.5	3.0 0.5	ns, Min
$T_{SMCSCCK}/T_{SMCKCS}$	CS_B Setup/Hold	3.0 0.5	3.0 0.5	3.0 0.5	ns, Min
$T_{SMCKW}/T_{SMWCK}$	RDWR_B Setup/Hold	8.0 0.5	8.0 0.5	8.0 0.5	ns, Min
$T_{SMCKBY}$	BUSY Propagation Delay	7.5	7.5	7.5	ns, Max
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required)	10	10	10	ns, Min
$T_{SMCO}$	CCLK to DATA out in readback	9.0	9.0	9.0	ns, Max
$T_{SMCKBY}$	CCLK to BUSY out in readback	7.5	7.5	7.5	ns, Max
$F_{SMCK}$	Maximum Frequency, master mode with respect to nominal CCLK.	100	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode with respect to nominal CCLK.	±50	±50	±50	%
<b>Boundary-Scan Port Timing Specifications</b>					
$T_{TAPTCK}$	TMS and TDI Setup time before TCK	1.0	1.0	1.0	ns, Min
$T_{TCKTAP}$	TMS and TDI Hold time after TCK	2.0	2.0	2.0	ns, Min
$T_{TCKTDO}$	TCK falling edge to TDO output valid	6	6	6	ns, Max

**Table 44: Configuration Switching Characteristics (Continued)**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
F <sub>TCK</sub>	Maximum configuration TCK clock frequency	66	66	66	MHz, Max
F <sub>TCKB</sub>	Maximum boundary-scan TCK clock frequency	66	66	66	MHz, Max
<b>BPI Master Flash Mode Programming Switching</b>					
T <sub>BPICCO</sub> <sup>(4)</sup>	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge	10	10	10	ns
T <sub>BPIDCC</sub> /T <sub>BPICCD</sub>	Setup/Hold on D[15:0] data input pins	3.0 0.5	3.0 0.5	3.0 0.5	ns
T <sub>INITADDR</sub>	Minimum period of initial ADDR[25:0] address cycles	3.0	3.0	3.0	CCLK cycles
<b>SPI Master Flash Mode Programming Switching</b>					
T <sub>SPIDCC</sub> /T <sub>SPIDCCD</sub>	DIN Setup/Hold before/after the rising CCLK edge	4.0 0.0	4.0 0.0	4.0 0.0	ns
T <sub>SPICCM</sub>	MOSI clock to out	10	10	10	ns
T <sub>SPICCF</sub>	FCS_B clock to out	10	10	10	ns
T <sub>FSINIT</sub> /T <sub>FSINITH</sub>	FS[2:0] to INIT_B rising edge Setup and Hold	2	2	2	μs
<b>CCLK Output (Master Modes)</b>					
T <sub>MCCKL</sub>	Master CCLK clock minimum Low time	3.0	3.0	3.0	ns, Min
T <sub>MCCKH</sub>	Master CCLK clock minimum High time	3.0	3.0	3.0	ns, Min
<b>CCLK Input (Slave Modes)</b>					
T <sub>SCCKL</sub>	Slave CCLK clock minimum Low time	2.0	2.0	2.0	ns, Min
T <sub>SCCKH</sub>	Slave CCLK clock minimum High time	2.0	2.0	2.0	ns, Min
<b>Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK</b>					
F <sub>DCK</sub>	Maximum frequency for DCLK	500	450	400	MHz
T <sub>DMCCK_DADDR</sub> /T <sub>DMCKC_DADDR</sub>	DADDR Setup/Hold	1.2 0.0	1.35 0.0	1.56 0.0	ns
T <sub>DMCCK_DI</sub> /T <sub>DMCKC_DI</sub>	DI Setup/Hold	1.2 0.0	1.35 0.0	1.56 0.0	ns
T <sub>DMCCK_DEN</sub> /T <sub>DMCKC_DEN</sub>	DEN Setup/Hold time	1.2 0.0	1.35 0.0	1.56 0.0	ns
T <sub>DMCCK_DWE</sub> /T <sub>DMCKC_DWE</sub>	DWE Setup/Hold time	1.2 0.0	1.35 0.0	1.56 0.0	ns
T <sub>DMCKO_DO</sub>	CLK to out of DO <sup>(3)</sup>	1.0	1.12	1.3	ns
T <sub>DMCKO_DRDY</sub> /T <sub>DMCKCO_DRDY</sub>	CLK to out of DRDY	1.0	1.12	1.3	ns

**Notes:**

1. Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
2. To support longer delays in configuration, use the design solutions described in [UG190: Virtex-5 User Guide](#).
3. DO will hold until next DRP operation.
4. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

## Clock Buffers and Networks

Table 45: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$T_{BCCCK\_CE}/T_{BCKKC\_CE}^{(1)}$	CE pins Setup/Hold	0.27 0.00	0.27 0.00	0.31 0.00	ns
$T_{BCCCK\_S}/T_{BCKKC\_S}^{(1)}$	S pins Setup/Hold	0.27 0.00	0.27 0.00	0.31 0.00	ns
$T_{BCKCO\_O}$	BUFGCTRL delay from I0/I1 to O	0.19	0.22	0.25	ns
$T_{BGCKO\_O}$	BUFG delay from I0 to O	0.19	0.22	0.25	ns
<b>Maximum Frequency</b>					
$F_{MAX}$	Global clock tree (BUFG) for LX30, LX30T, LX50, LX50T, LX85, LX85T, LX110, LX110T, SX35T, and SX50T devices	710	650	600	MHz
$F_{MAX}$	Global clock tree (BUFG) for LX220, LX220T, LX330, LX330T, and SX95T devices	N/A	500	450	MHz

**Notes:**

- $T_{BCCCK\_CE}$  and  $T_{BCKKC\_CE}$  must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX\_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.

Table 46: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$T_{BUFIOCKO\_O}$	Clock to out delay from I to O	1.08	1.16	1.29	ns
<b>Maximum Frequency</b>					
$F_{MAX}$	I/O clock tree (BUFIO)	710	710	644	MHz

Table 47: Regional Clock Switching Characteristics (BUFR)

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$T_{BRCKO\_O}$	Clock to out delay from I to O	0.56	0.59	0.67	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.23	0.24	0.26	ns
$T_{BRDO\_CLRO}$	Propagation delay from CLR to O	0.61	0.70	0.82	ns
<b>Maximum Frequency</b>					
$F_{MAX}$	Regional clock tree (BUFR)	300	250	250	MHz

## PLL Specification

**Table 48: PLL Specification**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
$F_{INMAX}$	Maximum Input Clock Frequency	710	710	645	MHz
$F_{INMIN}$	Minimum Input Clock Frequency	19	19	19	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	<20% of clock input period or 1 ns Max			
$F_{INDUTY}$	Allowable Input Duty Cycle: 19—49 MHz	25/75			%
	Allowable Input Duty Cycle: 50—199 MHz	30/70			%
	Allowable Input Duty Cycle: 200—399 MHz	35/65			%
	Allowable Input Duty Cycle: 400—499 MHz	40/60			%
	Allowable Input Duty Cycle: >500 MHz	45/55			%
$F_{VCOMIN}$	Minimum PLL VCO Frequency	400	400	400	MHz
$F_{VCOMAX}$	Maximum PLL VCO Frequency	1440	1200	1000	MHz
$F_{BANDWIDTH}$	Low PLL Bandwidth at Typical	1	1	1	MHz
	High PLL Bandwidth at Typical	4	4	4	MHz
$T_{STAPHAOFFSET}$	Static Phase Offset of the PLL Outputs	120	120	120	ps
$T_{OUTJITTER}$	PLL Output Jitter <sup>(1)</sup>	Note 1			
$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision <sup>(2)</sup>	150	200	200	ps
$T_{LOCKMAX}$	PLL Maximum Lock Time <sup>(4)</sup>	100	100	100	μs
$F_{OUTMAX}$	PLL Maximum Output Frequency for LX30, LX30T, LX50, LX50T, LX85, LX85T, LX110, LX110T, SX35T, and SX50T devices	710	650	600	MHz
	PLL Maximum Output Frequency for LX220, LX220T, LX330, LX330T, and SX95T devices	N/A	500	450	MHz
$F_{OUTMIN}$	PLL Minimum Output Frequency <sup>(3)</sup>	3.125	3.125	3.125	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	<20% of clock input period or 1 ns Max			
$RST_{MINPULSE}$	Minimum Reset Pulse Width	5	5	5	ns
$F_{PFDMAX}$	Maximum Frequency at the Phase Frequency Detector	550	500	450	MHz
$F_{PFDMIN}$	Minimum Frequency at the Phase Frequency Detector	19	19	19	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle			

**Notes:**

1. Values for this parameter are available in the Architecture Wizard.
2. Includes global clock buffer.
3. Calculated as  $F_{VCO}/128$  assuming output duty cycle is 50%.
4. The LOCK signal must be sampled after TLOCKMAX. The LOCK signal is invalid after configuration or reset until the TLOCKMAX time has expired.

## DCM Switching Characteristics

Table 49: Operating Frequency Ranges for DCM in Maximum Speed (MS) Mode

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Outputs Clocks (Low Frequency Mode)</b>					
F <sub>1XLFMSMIN</sub>	CLK0, CLK90, CLK180, CLK270	32.00	32.00	32.00	MHz
F <sub>1XLFMSMAX</sub>		150.00	135.00	120.00	MHz
F <sub>2XLFMSMIN</sub>	CLK2X, CLK2X180	64.00	64.00	64.00	MHz
F <sub>2XLFMSMAX</sub>		300.00	270.00	240.00	MHz
F <sub>DVLFMSMIN</sub>	CLKDV	2.0	2.0	2.0	MHz
F <sub>DVLFMSMAX</sub>		100.00	90.00	80.00	MHz
F <sub>FXLFMSMIN</sub>	CLKFX, CLKFX180	32.00	32.00	32.00	MHz
F <sub>FXLFMSMAX</sub>		180.00	160.00	140.00	MHz
<b>Input Clocks (Low Frequency Mode)</b>					
F <sub>DLLLFMSMIN</sub>	CLKIN (using DLL outputs) <sup>(1, 3, 4)</sup>	32.00	32.00	32.00	MHz
F <sub>DLLLFMSMAX</sub>		150.00	135.00	120.00	MHz
F <sub>CLKINLFFXMSMIN</sub>	CLKIN (using DFS outputs only) <sup>(2, 3, 4)</sup>	1.00	1.00	1.00	MHz
F <sub>CLKINLFFXMSMAX</sub>		180.00	160.00	140.00	MHz
F <sub>PSCLKLFMSMIN</sub>	PSCLK	1.00	1.00	1.00	KHz
F <sub>PSCLKLFMSMAX</sub>		550.00	500.00	450.00	MHz
<b>Outputs Clocks (High Frequency Mode)</b>					
F <sub>1XHFMSMIN</sub>	CLK0, CLK90, CLK180, CLK270	120.00	120.00	120.00	MHz
F <sub>1XHFMSMAX</sub>		550.00	500.00	450.00	MHz
F <sub>2XHFMSMIN</sub>	CLK2X, CLK2X180	240.00	240.00	240.00	MHz
F <sub>2XHFMSMAX</sub>		550.00	500.00	450.00	MHz
F <sub>DVHFMSMIN</sub>	CLKDV	7.5	7.5	7.5	MHz
F <sub>DVHFMSMAX</sub>		366.67	333.34	300.00	MHz
F <sub>FXHFMSMIN</sub>	CLKFX, CLKFX180	140.00	140.00	140.00	MHz
F <sub>FXHFMSMAX</sub>		400.00	375.00	350.00	MHz
<b>Input Clocks (High Frequency Mode)</b>					
F <sub>DLLHFMSMIN</sub>	CLKIN (using DLL outputs) <sup>(1, 3, 4)</sup>	120.00	120.00	120.00	MHz
F <sub>DLLHFMSMAX</sub>		550.00	500.00	450.00	MHz
F <sub>CLKINHFFXMSMIN</sub>	CLKIN (using DFS outputs only) <sup>(2, 3, 4)</sup>	25.00	25.00	25.00	MHz
F <sub>CLKINHFFXMSMAX</sub>		400.00	375.00	350.00	MHz
F <sub>PSCLKHFMSMIN</sub>	PSCLK	1.00	1.00	1.00	KHz
F <sub>PSCLKHFMSMAX</sub>		550.00	500.00	450.00	MHz

**Notes:**

1. DLL outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. When using the DCMs CLKIN\_DIVIDE\_BY\_2 attribute these values should be doubled. Other resources can limit the maximum input frequency.
4. When using a CLKIN frequency > 400 MHz and the DCMs CLKIN\_DIVIDE\_BY\_2 attribute, the CLKIN duty cycle must be within ±5% (45/55 to 55/45).

Table 50: Operating Frequency Ranges for DCM in Maximum Range (MR) Mode

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Outputs Clocks (Low Frequency Mode)</b>					
F <sub>1XMRMIN</sub>	CLK0, CLK90, CLK180, CLK270	19.00	19.00	19.00	MHz
F <sub>1XMRMAX</sub>		32.00	32.00	32.00	MHz
F <sub>2XMRMIN</sub>	CLK2X, CLK2X180	38.00	38.00	38.00	MHz
F <sub>2XMRMAX</sub>		64.00	64.00	64.00	MHz
F <sub>DLLMRMIN</sub>	CLKDV	1.19	1.19	1.19	MHz
F <sub>DLLMRMAX</sub>		21.34	21.34	21.34	MHz
F <sub>FXMRMIN</sub>	CLKFX, CLKFX180	19.00	19.00	19.00	MHz
F <sub>FXMRMAX</sub>		40.00	40.00	40.00	MHz
<b>Input Clocks (Low Frequency Mode)</b>					
F <sub>CLKINDLLMRMIN</sub>	CLKIN (using DLL outputs) <sup>(1, 3, 4)</sup>	19.00	19.00	19.00	MHz
F <sub>CLKINDLLMRMAX</sub>		32.00	32.00	32.00	MHz
F <sub>CLKINFXMRMIN</sub>	CLKIN (using DFS outputs only) <sup>(2, 3, 4)</sup>	1.00	1.00	1.00	MHz
F <sub>CLKINFXMRMAX</sub>		40.00	40.00	40.00	MHz
F <sub>PSCLKMRMIN</sub>	PSCLK	1.00	1.00	1.00	KHz
F <sub>PSCLKMRMAX</sub>		300.00	270.00	240.00	MHz

**Notes:**

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. When using the DCMs CLKIN\_DIVIDE\_BY\_2 attribute these values should be doubled. Other resources can limit the maximum input frequency.
4. When using a CLKIN frequency > 400 MHz and the DCMs CLKIN\_DIVIDE\_BY\_2 attribute, the CLKIN duty cycle must be within ±5% (45/55 to 55/45).



**Table 51: Input Clock Tolerances**

Symbol	Description	Frequency Range		Value	Units
<b>Duty Cycle Input Tolerance (in %)</b>					
T <sub>DUTYCYCRANGE_1</sub>	PSCLK only	< 1 MHz		25 - 75	%
T <sub>DUTYCYCRANGE_1_50</sub>	PSCLK and CLKIN	1 - 50 MHz		25 - 75	%
T <sub>DUTYCYCRANGE_50_100</sub>		50 - 100 MHz		30 - 70	%
T <sub>DUTYCYCRANGE_100_200</sub>		100 - 200 MHz		40 - 60	%
T <sub>DUTYCYCRANGE_200_400</sub>		200 - 400 MHz <sup>(4)</sup>		45 - 55	%
T <sub>DUTYCYCRANGE_400</sub>		> 400 MHz		45 - 55	%
		<b>Speed Grade</b>			
<b>Input Clock Cycle-Cycle Jitter (Low Frequency Mode)</b>		<b>-3</b>	<b>-2</b>	<b>-1</b>	<b>Units</b>
T <sub>CYCLFDLL</sub>	CLKIN (using DLL outputs) <sup>(1)</sup>	300.00	300.00	345.00	ps
T <sub>CYCLFFX</sub>	CLKIN (using DFS outputs) <sup>(2)</sup>	300.00	300.00	345.00	ps
<b>Input Clock Cycle-Cycle Jitter (High Frequency Mode)</b>					
T <sub>CYCHFDLL</sub>	CLKIN (using DLL outputs) <sup>(1)</sup>	150.00	150.00	173.00	ps
T <sub>CYCHFFX</sub>	CLKIN (using DFS outputs) <sup>(2)</sup>	150.00	150.00	173.00	ps
<b>Input Clock Period Jitter (Low Frequency Mode)</b>					
T <sub>PERLFDLL</sub>	CLKIN (using DLL outputs) <sup>(1)</sup>	1.00	1.00	1.15	ns
T <sub>PERLFFX</sub>	CLKIN (using DFS outputs) <sup>(2)</sup>	1.00	1.00	1.15	ns
<b>Input Clock Period Jitter (High Frequency Mode)</b>					
T <sub>PERHFDLL</sub>	CLKIN (using DLL outputs) <sup>(1)</sup>	1.00	1.00	1.15	ns
T <sub>PERHFFX</sub>	CLKIN (using DFS outputs) <sup>(2)</sup>	1.00	1.00	1.15	ns
<b>Feedback Clock Path Delay Variation</b>					
T <sub>CLKFB_DELAY_VAR</sub>	CLKFB off-chip feedback	1.00	1.00	1.15	ns

**Notes:**

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. If both DLL and DFS outputs are used, follow the more restrictive specifications.
4. This duty cycle specification does not apply to the GTP\_DUAL to DCM connection. The GTP transceivers drive the DCMs at the following frequencies: 320 MHz for -1 speed grade devices, 375 MHz for -2 speed grade devices, or 375 MHz for -3 speed grade devices.

## Output Clock Jitter

Table 52: Output Clock Jitter

Symbol	Description	Constraints	Speed Grade			Units
			-3	-2	-1	
<b>Clock Synthesis Period Jitter</b>						
T <sub>PERJITT_0</sub>	CLK0		±120	±120	±120	ps
T <sub>PERJITT_90</sub>	CLK90		±120	±120	±120	ps
T <sub>PERJITT_180</sub>	CLK180		±120	±120	±120	ps
T <sub>PERJITT_270</sub>	CLK270		±120	±120	±120	ps
T <sub>PERJITT_2X</sub>	CLK2X, CLK2X180		±200	±200	±230	ps
T <sub>PERJITT_DV1</sub>	CLKDV (integer division)		±150	±150	±180	ps
T <sub>PERJITT_DV2</sub>	CLKDV (non-integer division)		±300	±300	±345	ps
T <sub>PERJITT_FX</sub>	CLKFX, CLKFX180		Note 1	Note 1	Note 1	ps

**Notes:**

- Values for this parameter are available in the Architecture Wizard.

## Output Clock Phase Alignment

Table 53: Output Clock Phase Alignment

Symbol	Description	Constraints	Speed Grade			Units
			-3	-2	-1	
<b>Phase Offset Between CLKIN and CLKFB</b>						
T <sub>IN_FB_OFFSET</sub>	CLKIN/CLKFB		±50	±50	±60	ps
<b>Phase Offset Between Any DCM Outputs<sup>(4)</sup></b>						
T <sub>OUT_OFFSET_1X</sub>	CLK0, CLK90, CLK180, CLK270		±140	±140	±160	ps
T <sub>OUT_OFFSET_2X</sub>	CLK2X, CLK2X180, CLKDV		±150	±150	±200	ps
T <sub>OUT_OFFSET_FX</sub>	CLKFX, CLKFX180		±160	±160	±220	ps
<b>Duty Cycle Precision</b>						
T <sub>DUTY_CYC_DLL</sub> <sup>(3)</sup>	DLL outputs <sup>(1)</sup>		±150	±150	±180	ps
T <sub>DUTY_CYC_FX</sub>	DFS outputs <sup>(2)</sup>		±150	±150	±180	ps

**Notes:**

- DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
- DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
- CLKOUT\_DUTY\_CYCLE\_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY\_CYCLE\_CORRECTION = TRUE.
- All phase offsets are in respect to group CLK1X.

**Table 54: Miscellaneous Timing Parameters**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Time Required to Achieve LOCK</b>					
T <sub>DLL_240</sub>	DLL output – Frequency range > 240 MHz <sup>(1)</sup>	80.00	80.00	80.00	μs
T <sub>DLL_120_240</sub>	DLL output – Frequency range 120 - 240 MHz <sup>(1)</sup>	250.00	250.00	250.00	μs
T <sub>DLL_60_120</sub>	DLL output – Frequency range 60 - 120 MHz <sup>(1)</sup>	900.00	900.00	900.00	μs
T <sub>DLL_50_60</sub>	DLL output – Frequency range 50 - 60 MHz <sup>(1)</sup>	1300.00	1300.00	1300.00	μs
T <sub>DLL_40_50</sub>	DLL output – Frequency range 40 - 50 MHz <sup>(1)</sup>	2000.00	2000.00	2000.00	μs
T <sub>DLL_30_40</sub>	DLL output – Frequency range 30 - 40 MHz <sup>(1)</sup>	3600.00	3600.00	3600.00	μs
T <sub>DLL_24_30</sub>	DLL output – Frequency range 24 - 30 MHz <sup>(1)</sup>	5000.00	5000.00	5000.00	μs
T <sub>DLL_30</sub>	DLL output – Frequency range < 30 MHz <sup>(1)</sup>	5000.00	5000.00	5000.00	μs
T <sub>FX_MIN</sub>	DFS outputs <sup>(2)</sup>	10.00	10.00	10.00	ms
T <sub>FX_MAX</sub>		10.00	10.00	10.00	ms
T <sub>DLL_FINE_SHIFT</sub>	Multiplication factor for DLL lock time with Fine Shift	2.00	2.00	2.00	
<b>Fine Phase Shifting</b>					
T <sub>RANGE_MS</sub>	Absolute shifting range in maximum speed mode	7.00	7.00	7.00	ns
T <sub>RANGE_MR</sub>	Absolute shifting range in maximum range mode	10.00	10.00	10.00	ns
<b>Delay Lines</b>					
T <sub>TAP_MS_MIN</sub>	Tap delay resolution (Min) in maximum speed mode	7.00	7.00	7.00	ps
T <sub>TAP_MS_MAX</sub>	Tap delay resolution (Max) in maximum speed mode	30.00	30.00	30.00	ps
T <sub>TAP_MR_MIN</sub>	Tap delay resolution (Min) in maximum range mode	10.00	10.00	10.00	ps
T <sub>TAP_MR_MAX</sub>	Tap delay resolution (Max) in maximum range mode	40.00	40.00	40.00	ps

**Notes:**

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.

**Table 55: Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY	2	33
CLKFX_DIVIDE	1	32

**Table 56: DCM Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
T <sub>DMCK_PSEN</sub> / T <sub>DMCK_PSEN</sub>	PSEN Setup/Hold	1.20 0.00	1.35 0.00	1.56 0.00	ns
T <sub>DMCK_PSINCDEC</sub> / T <sub>DMCK_PSINCDEC</sub>	PSINCDEC Setup/Hold	1.20 0.00	1.35 0.00	1.56 0.00	ns
T <sub>DMCKO_PSDONE</sub>	Clock to out of PSDONE	1.00	1.12	1.30	ns

## Virtex-5 Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in [Table 57](#). Values are expressed in nanoseconds unless otherwise noted.

**Table 57: Global Clock Input to Output Delay Without DCM or PLL**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
LVC MOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>without</i> DCM or PLL						
T <sub>ICKOF</sub>	Global Clock and OUTFF <i>without</i> DCM or PLL	XC5VLX30	5.54	6.04	6.73	ns
		XC5VLX30T	5.54	6.04	6.73	ns
		XC5VLX50	5.59	6.09	6.79	ns
		XC5VLX50T	5.59	6.09	6.79	ns
		XC5VLX85	5.78	6.28	6.99	ns
		XC5VLX85T	5.78	6.28	6.99	ns
		XC5VLX110	5.84	6.35	7.06	ns
		XC5VLX110T	5.84	6.35	7.06	ns
		XC5VLX220	N/A	6.99	7.71	ns
		XC5VLX220T	N/A	6.99	7.71	ns
		XC5VLX330	N/A	7.17	7.91	ns
		XC5VLX330T	N/A	7.17	7.91	ns
		XC5VSX35T	5.72	6.22	6.92	ns
		XC5VSX50T	5.77	6.27	6.97	ns
		XC5VSX95T	N/A	6.59	7.30	ns

**Notes:**

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

**Table 58: Global Clock Input to Output Delay With DCM in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in System-Synchronous Mode.						
T <sub>ICKOFDCM</sub>	Global Clock and OUTFF <i>with</i> DCM	XC5VLX30	2.33	2.56	2.93	ns
		XC5VLX30T	2.33	2.56	2.93	ns
		XC5VLX50	2.35	2.58	2.95	ns
		XC5VLX50T	2.35	2.58	2.95	ns
		XC5VLX85	2.41	2.63	3.00	ns
		XC5VLX85T	2.41	2.63	3.00	ns
		XC5VLX110	2.46	2.69	3.06	ns
		XC5VLX110T	2.46	2.69	3.06	ns
		XC5VLX220	N/A	2.83	3.18	ns
		XC5VLX220T	N/A	2.83	3.18	ns
		XC5VLX330	N/A	3.00	3.37	ns
		XC5VLX330T	N/A	3.00	3.37	ns
		XC5VSX35T	2.44	2.67	3.03	ns
		XC5VSX50T	2.46	2.69	3.05	ns
		XC5VSX95T	N/A	2.64	3.00	ns

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

**Table 59: Global Clock Input to Output Delay With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
LVC MOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in Source-Synchronous Mode.						
T <sub>ICKOFDCM_0</sub>	Global Clock and OUTFF <i>with</i> DCM	XC5VLX30	3.45	3.71	4.15	ns
		XC5VLX30T	3.45	3.71	4.15	ns
		XC5VLX50	3.47	3.73	4.17	ns
		XC5VLX50T	3.47	3.73	4.17	ns
		XC5VLX85	3.60	3.86	4.29	ns
		XC5VLX85T	3.60	3.86	4.29	ns
		XC5VLX110	3.65	3.92	4.36	ns
		XC5VLX110T	3.65	3.92	4.36	ns
		XC5VLX220	N/A	4.41	4.85	ns
		XC5VLX220T	N/A	4.41	4.85	ns
		XC5VLX330	N/A	4.58	5.04	ns
		XC5VLX330T	N/A	4.58	5.04	ns
		XC5VSX35T	3.63	3.89	4.33	ns
		XC5VSX50T	3.65	3.91	4.35	ns
		XC5VSX95T	N/A	4.16	4.59	ns

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

**Table 60: Global Clock Input to Output Delay With PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
LVC MOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in System-Synchronous Mode.						
T <sub>ICKOFFPLL</sub>	Global Clock and OUTFF <i>with</i> PLL	XC5VLX30	2.03	2.12	2.41	ns
		XC5VLX30T	2.03	2.12	2.41	ns
		XC5VLX50	2.05	2.14	2.43	ns
		XC5VLX50T	2.05	2.14	2.43	ns
		XC5VLX85	2.10	2.18	2.47	ns
		XC5VLX85T	2.10	2.18	2.47	ns
		XC5VLX110	2.16	2.24	2.54	ns
		XC5VLX110T	2.16	2.24	2.54	ns
		XC5VLX220	N/A	2.58	2.86	ns
		XC5VLX220T	N/A	2.58	2.86	ns
		XC5VLX330	N/A	2.75	3.05	ns
		XC5VLX330T	N/A	2.75	3.05	ns
		XC5VSX35T	2.14	2.22	2.51	ns
		XC5VSX50T	2.16	2.24	2.53	ns
XC5VSX95T	N/A	2.32	2.60	ns		

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

**Table 61: Global Clock Input to Output Delay With PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
LVC MOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in Source-Synchronous Mode.						
T <sub>ICKOFFPLL_0</sub>	Global Clock and OUTFF <i>with</i> PLL	XC5VLX30	3.98	4.33	4.82	ns
		XC5VLX30T	3.98	4.33	4.82	ns
		XC5VLX50	4.01	4.35	4.84	ns
		XC5VLX50T	4.01	4.35	4.84	ns
		XC5VLX85	4.13	4.47	4.96	ns
		XC5VLX85T	4.13	4.47	4.96	ns
		XC5VLX110	4.19	4.53	5.03	ns
		XC5VLX110T	4.19	4.53	5.03	ns
		XC5VLX220	N/A	5.03	5.53	ns
		XC5VLX220T	N/A	5.03	5.53	ns
		XC5VLX330	N/A	5.20	5.71	ns
		XC5VLX330T	N/A	5.20	5.71	ns
		XC5VSX35T	4.16	4.51	5.00	ns
		XC5VSX50T	4.19	4.53	5.02	ns
		XC5VSX95T	N/A	4.77	5.27	ns

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.



**Table 62: Global Clock Input to Output Delay With DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
LVC MOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM and PLL in System-Synchronous Mode.						
T <sub>ICKOFDCM_PLL</sub>	Global Clock and OUTFF with DCM and PLL	XC5VLX30	2.47	2.70	3.06	ns
		XC5VLX30T	2.47	2.70	3.06	ns
		XC5VLX50	2.49	2.72	3.08	ns
		XC5VLX50T	2.49	2.72	3.08	ns
		XC5VLX85	2.55	2.77	3.13	ns
		XC5VLX85T	2.55	2.77	3.13	ns
		XC5VLX110	2.60	2.83	3.19	ns
		XC5VLX110T	2.60	2.83	3.19	ns
		XC5VLX220	N/A	2.97	3.31	ns
		XC5VLX220T	N/A	2.97	3.31	ns
		XC5VLX330	N/A	3.14	3.49	ns
		XC5VLX330T	N/A	3.14	3.49	ns
		XC5VSX35T	2.58	2.81	3.16	ns
		XC5VSX50T	2.60	2.83	3.18	ns
		XC5VSX95T	N/A	2.78	3.13	ns

**Notes:**

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
- DCM and PLL output jitter are already included in the timing calculation.

**Table 63: Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
LVC MOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM and PLL in Source-Synchronous Mode.						
T <sub>ICKOFDCM0_PLL</sub>	Global Clock and OUTFF with DCM and PLL	XC5VLX30	3.59	3.85	4.27	ns
		XC5VLX30T	3.59	3.85	4.27	ns
		XC5VLX50	3.61	3.87	4.29	ns
		XC5VLX50T	3.61	3.87	4.29	ns
		XC5VLX85	3.74	4.00	4.42	ns
		XC5VLX85T	3.74	4.00	4.42	ns
		XC5VLX110	3.79	4.06	4.48	ns
		XC5VLX110T	3.79	4.06	4.48	ns
		XC5VLX220	N/A	4.55	4.98	ns
		XC5VLX220T	N/A	4.55	4.98	ns
		XC5VLX330	N/A	4.72	5.17	ns
		XC5VLX330T	N/A	4.72	5.17	ns
		XC5VSX35T	3.77	4.03	4.45	ns
		XC5VSX50T	3.79	4.05	4.48	ns
		XC5VSX95T	N/A	4.30	4.72	ns

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

## Virtex-5 Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in [Table 65](#). Values are expressed in nanoseconds unless otherwise noted.

**Table 64: Global Clock Setup and Hold Without DCM or PLL**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
<b>Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.<sup>(1)</sup></b>						
T <sub>PSFD</sub> / T <sub>PHFD</sub>	Full Delay (Legacy Delay or Default Delay) Global Clock and IFF <sup>(2)</sup> without DCM or PLL	XC5VLX30	1.49 -0.35	1.60 -0.35	1.77 -0.35	ns
		XC5VLX30T	1.49 -0.35	1.60 -0.35	1.76 -0.35	ns
		XC5VLX50	1.48 -0.30	1.59 -0.30	1.76 -0.30	ns
		XC5VLX50T	1.48 -0.30	1.59 -0.30	1.76 -0.30	ns
		XC5VLX85	1.75 -0.49	1.89 -0.49	2.09 -0.49	ns
		XC5VLX85T	1.75 -0.49	1.89 -0.49	2.09 -0.49	ns
		XC5VLX110	1.74 -0.43	1.88 -0.43	2.09 -0.43	ns
		XC5VLX110T	1.73 -0.43	1.88 -0.43	2.09 -0.43	ns
		XC5VLX220	N/A	2.57 -0.74	2.86 -0.74	ns
		XC5VLX220T	N/A	2.57 -0.74	2.86 -0.74	ns
		XC5VLX330	N/A	2.55 -0.56	2.85 -0.56	ns
		XC5VLX330T	N/A	2.57 -0.56	2.86 -0.56	ns
		XC5VSX35T	1.47 -0.16	1.59 -0.16	1.76 -0.16	ns
		XC5VSX50T	1.62 -0.31	1.74 -0.31	1.93 -0.31	ns
		XC5VSX95T	N/A	2.10 -0.44	2.32 -0.44	ns

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

**Table 65: Global Clock Setup and Hold With DCM in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
<b>Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.<sup>(1)</sup></b>						
T <sub>PSDCM</sub> / T <sub>PHDCM</sub>	No Delay Global Clock and IFF <sup>(2)</sup> with DCM in System-Synchronous Mode	XC5VLX30	1.53 -0.50	1.70 -0.50	1.88 -0.50	ns
		XC5VLX30T	1.53 -0.50	1.70 -0.50	1.88 -0.50	ns
		XC5VLX50	1.52 -0.48	1.68 -0.48	1.86 -0.48	ns
		XC5VLX50T	1.52 -0.48	1.68 -0.48	1.86 -0.48	ns
		XC5VLX85	1.58 -0.43	1.76 -0.43	1.95 -0.43	ns
		XC5VLX85T	1.57 -0.43	1.76 -0.43	1.95 -0.43	ns
		XC5VLX110	1.58 -0.37	1.76 -0.37	1.95 -0.37	ns
		XC5VLX110T	1.58 -0.37	1.76 -0.37	1.95 -0.37	ns
		XC5VLX220	N/A	2.17 -0.27	2.44 -0.27	ns
		XC5VLX220T	N/A	2.17 -0.27	2.44 -0.27	ns
		XC5VLX330	N/A	2.17 -0.10	2.44 -0.10	ns
		XC5VLX330T	N/A	2.17 -0.10	2.44 -0.10	ns
		XC5VSX35T	1.60 -0.39	1.78 -0.39	1.98 -0.39	ns
		XC5VSX50T	1.58 -0.37	1.76 -0.37	1.95 -0.37	ns
		XC5VSX95T	N/A	2.10 -0.41	2.35 -0.41	ns

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CLK0, DCM, and jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

**Table 66: Global Clock Setup and Hold With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
<b>Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.<sup>(1)</sup></b>						
$T_{PSDCM0}$ / $T_{PHDCM0}$	No Delay Global Clock and IFF <sup>(2)</sup> with DCM in Source-Synchronous Mode	XC5VLX30	0.27 0.62	0.27 0.62	0.27 0.66	ns
		XC5VLX30T	0.27 0.62	0.27 0.62	0.27 0.66	ns
		XC5VLX50	0.26 0.64	0.26 0.64	0.26 0.68	ns
		XC5VLX50T	0.25 0.64	0.26 0.64	0.26 0.68	ns
		XC5VLX85	0.23 0.76	0.24 0.76	0.24 0.80	ns
		XC5VLX85T	0.23 0.76	0.24 0.76	0.24 0.80	ns
		XC5VLX110	0.23 0.82	0.24 0.82	0.24 0.87	ns
		XC5VLX110T	0.23 0.82	0.24 0.82	0.24 0.87	ns
		XC5VLX220	N/A	0.21 1.31	0.22 1.36	ns
		XC5VLX220T	N/A	0.21 1.31	0.22 1.36	ns
		XC5VLX330	N/A	0.21 1.48	0.22 1.55	ns
		XC5VLX330T	N/A	0.21 1.48	0.22 1.55	ns
		XC5VSX35T	0.25 0.80	0.27 0.80	0.27 0.84	ns
		XC5VSX50T	0.24 0.82	0.25 0.82	0.25 0.86	ns
		XC5VSX95T	N/A	0.24 1.06	0.24 1.11	ns

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CLK0, DCM, and jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

**Table 67: Global Clock Setup and Hold With PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
<b>Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.<sup>(1)</sup></b>						
T <sub>PSPLL</sub> /T <sub>PHPLL</sub>	No Delay Global Clock and IFF <sup>(2)</sup> with PLL in System-Synchronous Mode	XC5VLX30	1.51 -0.81	1.67 -0.81	1.91 -0.81	ns
		XC5VLX30T	1.51 -0.81	1.67 -0.81	1.91 -0.81	ns
		XC5VLX50	1.49 -0.79	1.65 -0.79	1.88 -0.79	ns
		XC5VLX50T	1.49 -0.79	1.65 -0.79	1.88 -0.79	ns
		XC5VLX85	1.52 -0.74	1.70 -0.74	1.95 -0.74	ns
		XC5VLX85T	1.52 -0.74	1.70 -0.74	1.95 -0.74	ns
		XC5VLX110	1.51 -0.68	1.69 -0.68	1.95 -0.68	ns
		XC5VLX110T	1.51 -0.68	1.69 -0.68	1.95 -0.68	ns
		XC5VLX220	N/A	1.77 -0.52	2.08 -0.52	ns
		XC5VLX220T	N/A	1.77 -0.52	2.08 -0.52	ns
		XC5VLX330	N/A	1.75 -0.35	2.07 -0.35	ns
		XC5VLX330T	N/A	1.77 -0.35	2.08 -0.35	ns
		XC5VSX35T	1.56 -0.70	1.73 -0.70	1.98 -0.70	ns
		XC5VSX50T	1.54 -0.68	1.71 -0.68	1.96 -0.68	ns
		XC5VSX95T	N/A	1.83 -0.58	2.11 -0.58	ns

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CLKOUT0, PLL, and jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

**Table 68: Global Clock Setup and Hold With PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
<b>Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.<sup>(1)</sup></b>						
$T_{PSPLL0} / T_{PHPLL0}$	No Delay Global Clock and IFF <sup>(2)</sup> with PLL in Source-Synchronous Mode	XC5VLX30	-0.21 1.15	-0.21 1.23	-0.21 1.33	ns
		XC5VLX30T	-0.21 1.15	-0.21 1.23	-0.21 1.33	ns
		XC5VLX50	-0.22 1.17	-0.22 1.25	-0.22 1.35	ns
		XC5VLX50T	-0.22 1.17	-0.22 1.25	-0.22 1.35	ns
		XC5VLX85	-0.24 1.29	-0.24 1.37	-0.24 1.48	ns
		XC5VLX85T	-0.24 1.29	-0.24 1.37	-0.24 1.48	ns
		XC5VLX110	-0.24 1.35	-0.24 1.43	-0.24 1.54	ns
		XC5VLX110T	-0.24 1.35	-0.24 1.43	-0.24 1.54	ns
		XC5VLX220	N/A	-0.31 1.93	-0.31 2.04	ns
		XC5VLX220T	N/A	-0.32 1.93	-0.32 2.04	ns
		XC5VLX330	N/A	-0.31 2.10	-0.31 2.22	ns
		XC5VLX330T	N/A	-0.32 2.10	-0.32 2.22	ns
		XC5VSX35T	-0.22 1.33	-0.22 1.41	-0.22 1.51	ns
		XC5VSX50T	-0.24 1.35	-0.24 1.43	-0.24 1.53	ns
		XC5VSX95T	N/A	-0.26 1.67	-0.26 1.78	ns

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CLKOUT0, PLL, and jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

**Table 69: Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
<b>Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.<sup>(1)</sup></b>						
$T_{PSDCMPLL}/$ $T_{PHDCMPLL}$	No Delay Global Clock and IFF <sup>(2)</sup> with DCM and PLL in System-Synchronous Mode	XC5VLX30	1.66 -0.37	1.83 -0.37	2.00 -0.37	ns
		XC5VLX30T	1.65 -0.37	1.83 -0.37	2.00 -0.37	ns
		XC5VLX50	1.63 -0.34	1.80 -0.34	1.98 -0.34	ns
		XC5VLX50T	1.63 -0.34	1.80 -0.34	1.98 -0.34	ns
		XC5VLX85	1.68 -0.29	1.87 -0.29	2.07 -0.29	ns
		XC5VLX85T	1.68 -0.29	1.87 -0.29	2.07 -0.29	ns
		XC5VLX110	1.67 -0.23	1.87 -0.23	2.07 -0.23	ns
		XC5VLX110T	1.66 -0.23	1.86 -0.23	2.06 -0.23	ns
		XC5VLX220	N/A	2.26 -0.13	2.55 -0.13	ns
		XC5VLX220T	N/A	2.25 -0.13	2.55 -0.13	ns
		XC5VLX330	N/A	2.23 0.04	2.53 0.04	ns
		XC5VLX330T	N/A	2.25 0.04	2.54 0.04	ns
		XC5VSX35T	1.72 -0.26	1.91 -0.26	2.10 -0.26	ns
		XC5VSX50T	1.70 -0.23	1.88 -0.23	2.07 -0.23	ns
		XC5VSX95T	N/A	2.22 -0.27	2.47 -0.27	ns

**Notes:**

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CLK0, DCM, CLKOUT0, PLL, and jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.



**Table 70: Global Clock Setup and Hold With DCM and PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
Example Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, <sup>(1)</sup> Using DCM, PLL, and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in <b>IOB Switching Characteristics</b> , page 23.						
T <sub>PSDCMPLL_0</sub> / T <sub>PHDCMPLL_0</sub>	No Delay Global Clock and IFF <sup>(2)</sup> with DCM and PLL in Source-Synchronous Mode	XC5VLX30	0.39 0.75	0.40 0.75	0.40 0.79	ns
		XC5VLX30T	0.39 0.75	0.40 0.75	0.40 0.79	ns
		XC5VLX50	0.37 0.78	0.38 0.78	0.38 0.81	ns
		XC5VLX50T	0.37 0.78	0.38 0.78	0.38 0.81	ns
		XC5VLX85	0.34 0.90	0.36 0.90	0.36 0.93	ns
		XC5VLX85T	0.33 0.90	0.36 0.90	0.36 0.93	ns
		XC5VLX110	0.32 0.96	0.35 0.96	0.35 1.00	ns
		XC5VLX110T	0.32 0.96	0.35 0.96	0.35 1.00	ns
		XC5VLX220	N/A	0.30 1.45	0.32 1.49	ns
		XC5VLX220T	N/A	0.30 1.45	0.32 1.49	ns
		XC5VLX330	N/A	0.28 1.62	0.31 1.68	ns
		XC5VLX330T	N/A	0.30 1.62	0.32 1.68	ns
		XC5VSX35T	0.38 0.93	0.39 0.93	0.39 0.97	ns
		XC5VSX50T	0.35 0.96	0.37 0.96	0.37 0.99	ns
		XC5VSX95T	N/A	0.35 1.20	0.35 1.24	ns

**Notes:**

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CLK0, DCM, CLKOUT0, PLL, and jitter. Package skew is not included in these measurements.
- IFF = Input Flip-Flop

## ChipSync™ Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-5 source-synchronous transmitter and receiver data-valid windows.

Table 71: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
$T_{DCD\_CLK}$	Global Clock Tree Duty Cycle Distortion <sup>(1)</sup>	All	0.12	0.12	0.12	ns
$T_{CKSKEW}$	Global Clock Tree Skew <sup>(2)</sup>	XC5VLX30	0.21	0.22	0.22	ns
		XC5VLX30T	0.21	0.22	0.22	ns
		XC5VLX50	0.26	0.27	0.28	ns
		XC5VLX50T	0.26	0.27	0.28	ns
		XC5VLX85	0.42	0.43	0.45	ns
		XC5VLX85T	0.42	0.43	0.45	ns
		XC5VLX110	0.48	0.50	0.51	ns
		XC5VLX110T	0.48	0.50	0.51	ns
		XC5VLX220	N/A	1.07	1.10	ns
		XC5VLX220T	N/A	1.07	1.10	ns
		XC5VLX330	N/A	1.25	1.29	ns
		XC5VLX330T	N/A	1.25	1.29	ns
		XC5VSX35T	0.38	0.39	0.39	ns
		XC5VSX50T	0.43	0.44	0.45	ns
		XC5VSX95T	N/A	0.72	0.74	ns
$T_{DCD\_BUFIO}$	I/O clock tree duty cycle distortion	All	0.10	0.10	0.10	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.07	0.07	0.08	ns
$T_{DCD\_BUFR}$	Regional clock tree duty cycle distortion	All	0.25	0.25	0.25	ns

**Notes:**

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The  $T_{CKSKEW}$  value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA\_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

**Table 72: Package Skew**

Symbol	Description	Device	Package	Value	Units
T <sub>PKGSKEW</sub>	Package Skew <sup>(1)</sup>	XC5VLX30	FF324	80	ps
			FF676	142	ps
		XC5VLX30T	FF665	93	ps
		XC5VLX50	FF324	80	ps
			FF676	142	ps
			FF1153	175	ps
		XC5VLX50T	FF665	93	ps
			FF1136	162	ps
		XC5VLX85	FF676	142	ps
			FF1153	174	ps
		XC5VLX85T	FF1136	164	ps
		XC5VLX110	FF676	142	ps
			FF1153	173	ps
			FF1760	190	ps
		XC5VLX110T	FF1136	163	ps
			FF1738	171	ps
		XC5VLX220	FF1760	178	ps
		XC5VLX220T	FF1738	156	ps
		XC5VLX330	FF1760	177	ps
		XC5VLX330T	FF1738	155	ps
XC5VSX35T	FF665	103	ps		
XC5VSX50T	FF665	103	ps		
	FF1136	157	ps		
XC5VSX95T	FF1136	176	ps		

**Notes:**

- These values represent the worst-case skew between any two SelectMap I/Os in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
- Package trace length information is available for these device/package combinations. This information can be used to deskew the package.

**Table 73: Sample Window**

Symbol	Description	Device	Speed Grade			Units
			-3	-2	-1	
T <sub>SAMP</sub>	Sampling Error at Receiver Pins <sup>(1)</sup>	All	450	500	550	ps
T <sub>SAMP_BUFIO</sub>	Sampling Error at Receiver Pins using BUFIO <sup>(2)</sup>	All	350	400	450	ps

**Notes:**

- This parameter indicates the total sampling error of Virtex-5 DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
  - CLK0 DCM jitter
  - DCM accuracy (phase offset)
  - DCM phase shift resolution
 These measurements do not include package or clock tree skew.
- This parameter indicates the total sampling error of Virtex-5 DDR input registers across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 74: ChipSync Pin-to-Pin Setup/Hold and Clock-to-Out

Symbol	Description	Speed Grade			Units
		-3	-2	-1	
<b>Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO</b>					
$T_{PSCS}/T_{PHCS}$	Setup/Hold of I/O clock	-0.56 1.59	-0.54 1.72	-0.54 1.91	ns
<b>Pin-to-Pin Clock-to-Out Using BUFIO</b>					
$T_{ICKOFCs}$	Clock-to-Out of I/O clock	4.42	4.82	5.40	ns

## Notice of Disclaimer

THE XILINX HARDWARE FPGA AND CPLD DEVICES REFERRED TO HEREIN ("PRODUCTS") ARE SUBJECT TO THE TERMS AND CONDITIONS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT <http://www.xilinx.com/warranty.htm>. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED IN THE XILINX DATA SHEET. ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE. PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, OR ANY OTHER APPLICATION THAT INVOKES THE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). USE OF PRODUCTS IN CRITICAL APPLICATIONS IS AT THE SOLE RISK OF CUSTOMER, SUBJECT TO APPLICABLE LAWS AND REGULATIONS.

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/14/06	1.0	Initial Xilinx release.
05/12/06	1.1	<ul style="list-style-type: none"> <li>First version posted to the Xilinx website. Minor typographical edits. Revised design software version on <a href="#">page 21</a>.</li> <li>Revised <math>T_{IDELAYRESOLUTION}</math> in <a href="#">Table 38, page 35</a>.</li> <li>Revised TDSPCKO in <a href="#">Table 43, page 40</a>.</li> </ul>
05/24/06	1.2	<ul style="list-style-type: none"> <li>Added register-to-register parameters to <a href="#">Table 26</a>.</li> </ul>
08/04/06	1.3	<ul style="list-style-type: none"> <li>Added <math>V_{DRINT}</math>, <math>V_{DRI}</math>, and <math>C_{IN}</math> values to <a href="#">Table 3</a>.</li> <li>Added HSTL_I_12 and LVCMOS12 to <a href="#">Table 7</a> and renumbered the notes.</li> <li>Removed pin-to-pin performance (Table 12). Updated and added values to register-register performance <a href="#">Table 26</a> (was Table 13).</li> <li>Added values to <a href="#">Table 27</a>.</li> <li>Updated the speed specification version above <a href="#">Table 28</a>.</li> <li>Added to <a href="#">Table 30</a> the I/O standards: HSTL_II_T_DCI, HSTL_II_T_DCI_18, SSTL2_II_T_DCI, and SSTL18_II_T_DCI.</li> <li>Revised <math>F_{MAX}</math> values in <a href="#">Table 42</a>, and RDWR_B Setup/Hold values in <a href="#">Table 44</a>.</li> <li>In <a href="#">Table 48</a>, changed <math>F_{VCOMAX}</math>, removed <math>T_{LOCKMIN}</math>, and revised <math>T_{LOCKMAX}</math> values, also removed note pointing to Architecture Wizard.</li> <li>Removed Note 2 on <a href="#">Table 61</a>.</li> </ul>
09/06/06	2.0	<ul style="list-style-type: none"> <li>Added new sections for LXT devices and added LXT devices to the appropriate tables. The addition of the <b>RocketIO GTP Transceiver Specifications</b> required the tables to be renumbered.</li> <li>Changed maximum <math>V_{IN}</math> values in <a href="#">Table 1</a> and <a href="#">Table 2</a>.</li> <li>Updated values and added <math>T_j = 85^{\circ}\text{C}</math> to <a href="#">Table 4, page 3</a>.</li> <li>Revised the cascade block RAM <b>Memory, page 19</b> section in <a href="#">Table 26</a> to 64K with new I/O delays.</li> <li>Revised the setup and hold times in <a href="#">Table 34, page 31</a>.</li> <li>Added <math>F_{MAX\_CASCADE}</math> to <a href="#">Table 42, page 38</a>.</li> <li>Revised <math>F_{FCLFMSMAX}</math> and <math>F_{CLKINLFFXMSMAX}</math> in <a href="#">Table 49, page 47</a>.</li> </ul>
10/13/06	2.1	<ul style="list-style-type: none"> <li>Added System Monitor parameters. Added XC5VLX85T to appropriate tables.</li> <li>Revised <a href="#">Table 16</a> including notes. Added <a href="#">Table 17</a>, and <a href="#">Figure 3</a> and <a href="#">Figure 4</a>.</li> <li>Added <a href="#">Table 19, page 14</a>: RocketIO CRC block.</li> <li>Revised design software version and <a href="#">Table 28</a> on <a href="#">page 21</a>.</li> <li>Updated <b>ILOGIC Switching Characteristics, page 31</b></li> <li>Updated <math>F_{MAX\_ECC}</math> in <a href="#">Table 42, page 38</a>.</li> <li>Changed hold times for <math>T_{SMDCC}/T_{SMCCD}</math> and <math>T_{BPIDCC}/T_{BPICD}</math> in <a href="#">Table 44, page 43</a>.</li> <li>Revised <math>T_{FBDELAY}</math>, <math>F_{OUTMIN}</math>, <math>F_{OUTMAX}</math>, and <math>F_{INJITTER}</math> <a href="#">Table 48, page 46</a>.</li> <li>Revised <a href="#">Table 49, page 47</a>.</li> </ul>

Date	Version	Revision
01/05/07	2.2	<ul style="list-style-type: none"> <li>• Added <math>I_{IN}</math> to <a href="#">Table 2</a>. Added XC5VLX220T to appropriate tables.</li> <li>• Added LVDCI33, LVDCI25, LVDCI18, LVDCI15 to <a href="#">Table 7</a>.</li> <li>• Update the symbols in the GTP Transceiver <a href="#">Table 12</a>, <a href="#">Table 13</a>, and <a href="#">Table 14</a>.</li> <li>• Add values for -1 speed grade in <a href="#">Table 18</a>, <a href="#">page 14</a>.</li> <li>• Added SFI-4.1 values to <a href="#">Table 27</a>, <a href="#">page 20</a>.</li> <li>• Removed -3 speed grade from available LX220 device list in <a href="#">Table 28</a>, <a href="#">page 21</a>.</li> <li>• Added maximum frequency to <a href="#">Table 46</a> and <a href="#">Table 47</a>, <a href="#">page 45</a>.</li> <li>• In <a href="#">Table 49</a>, <a href="#">page 47</a> changed the all the CLKDV, CLKFX, and CLKFX180 Min values and the CLKIN Min values in the Input Clocks (High Frequency Mode) section.</li> <li>• Added values to <a href="#">Table 52</a> and <a href="#">Table 53</a>, <a href="#">page 50</a>.</li> </ul>
02/02/07	3.0	<ul style="list-style-type: none"> <li>• Added XC5VSX35T, XC5VSX50T, and SX5VSX95T devices to appropriate tables.</li> <li>• Revised the <math>I_{RPJ}</math> values in <a href="#">Table 3</a>, <a href="#">page 2</a>.</li> <li>• Revised the <math>I_{CCAUXQ}</math> values in <a href="#">Table 4</a>, <a href="#">page 3</a>.</li> <li>• Added values to <a href="#">Table 5</a>, <a href="#">page 4</a>.</li> <li>• Minor added notes and changed descriptions in <a href="#">Table 13</a>, <a href="#">page 9</a> and <a href="#">Table 14</a>, <a href="#">page 9</a>.</li> <li>• Revised the SFI-4.1 (SDR LVDS Interface) -1 values in <a href="#">Table 27</a>, <a href="#">page 20</a>.</li> <li>• Revised gain error, bipolar gain error, and event conversion time in <a href="#">Table 25</a>, <a href="#">page 17</a></li> <li>• Changed the design software version that matches this datasheet above <a href="#">Table 28</a> on <a href="#">page 21</a>.</li> <li>• In <b>Switching Characteristics</b>, the following values are revised: <ul style="list-style-type: none"> <li>- LVCMOS25, Fast, 12 mA in <a href="#">Table 30</a>, <a href="#">page 23</a>.</li> <li>- Setup and Hold and <math>T_{ICKQ}</math> in <a href="#">Table 34</a>, <a href="#">page 31</a>.</li> <li>- <math>T_{OCKQ}</math> in <a href="#">Table 35</a>, <a href="#">page 32</a>.</li> <li>- Sequential delay values in <a href="#">Table 37</a>, <a href="#">page 34</a>.</li> <li>- <math>T_{CXB}</math>, <math>T_{CEO}</math>, and <math>T_{DICK}</math> in <a href="#">Table 39</a>, <a href="#">page 35</a>.</li> <li>- <math>T_{RCKO\_DO}</math>, <math>T_{RCKO\_POINTERS}</math>, <math>T_{RCKO\_ECCR}</math>, <math>T_{RCKO\_ECC}</math>, <math>T_{RCCK\_ADDR}</math>, <math>T_{RDCK\_DI}</math>, <math>T_{RDCK\_DI\_ECC}</math>, <math>T_{RCCK\_WREN}</math>, and <math>T_{RCO\_FLAGS}</math> in <a href="#">Table 42</a>, <a href="#">page 38</a>.</li> <li>- <math>T_{DSPDCK\_CC}</math>, <math>T_{DSPCCK\_RSTAA}</math>, <math>T_{DSPCCK\_RSTBB}</math>, <math>T_{DSPCKO\_PP\_CRYOUTP}</math>, <math>F_{MAX\_MULT\_NOMREG}</math> and <math>F_{MAX\_MULT\_NOMREG\_PATDET}</math> in <a href="#">Table 43</a>, <a href="#">page 40</a>.</li> <li>- <math>T_{BCCKO\_O}</math>, and <math>T_{BGCKO\_O}</math> in <a href="#">Table 45</a>, <a href="#">page 45</a>.</li> <li>- <math>T_{BUFIOCKO\_O}</math> and <math>F_{MAX}</math> in <a href="#">Table 46</a>, <a href="#">page 45</a>.</li> <li>- <math>T_{BRCKO\_O}</math> and <math>T_{BRCKO\_O\_BYP}</math> in <a href="#">Table 47</a>, <a href="#">page 45</a>.</li> <li>- Parameters in <a href="#">Table 48</a>, <a href="#">page 46</a> including notes.</li> </ul> </li> <li>• In <b>Virtex-5 Pin-to-Pin Output Parameter Guidelines</b>: <ul style="list-style-type: none"> <li>- Revised values in <a href="#">Table 57</a>, <a href="#">Table 58</a>, and <a href="#">Table 59</a>.</li> </ul> </li> <li>• In <b>Virtex-5 Pin-to-Pin Input Parameter Guidelines</b>: <ul style="list-style-type: none"> <li>- Clarified description in <a href="#">Table 64</a>, <a href="#">page 59</a>.</li> <li>- Revised values in <a href="#">Table 64</a>, <a href="#">Table 65</a>, and <a href="#">Table 66</a>.</li> <li>- Removed duplicate <math>T_{BUFR\_MAX\_FREQ}</math> and <math>T_{BUFIO\_MAX\_FREQ}</math> from <a href="#">Table 71</a>.</li> </ul> </li> <li>• Revised values in <a href="#">Table 74</a>, <a href="#">page 68</a>.</li> </ul>

Date	Version	Revision
05/18/07	3.1	<ul style="list-style-type: none"> <li>• Added typical values for n and r in <a href="#">Table 3</a>.</li> <li>• Revised and added values to <a href="#">Table 4</a>.</li> <li>• Revised standard I/O levels in <a href="#">Table 7</a>.</li> <li>• Additions and updates to <a href="#">Table 14</a>, <a href="#">Table 16</a>, <a href="#">Table 17</a>, <a href="#">Table 18</a>, <a href="#">Table 19</a>, <a href="#">Table 20</a>, <a href="#">Table 21</a>, <a href="#">Table 22</a>, and <a href="#">Table 23</a>.</li> <li>• Added <b>Ethernet MAC Switching Characteristics</b>, page 16.</li> <li>• Changed the design software version that matches this datasheet above <a href="#">Table 28</a> on <a href="#">page 21</a>.</li> <li>• Added new section: <b>I/O Standard Adjustment Measurement Methodology</b>, page 28.</li> <li>• In <b>Switching Characteristics</b>, the following values are revised:                         <ul style="list-style-type: none"> <li>- LVTTTL, Slow and Fast, 2 mA, 4 mA, and 6 mA (<a href="#">Table 30</a>).</li> <li>- LVC MOS33, Slow and Fast, 2 mA, 4 mA, and 6 mA (<a href="#">Table 30</a>).</li> <li>- LVC MOS25, Slow and Fast, 2 mA and 4 mA, and Fast 12 mA (<a href="#">Table 30</a>).</li> <li>- LVC MOS18, Slow and Fast, 2 mA, 4 mA, and 6 mA (<a href="#">Table 30</a>).</li> <li>- LVC MOS15 and LVC MOS12, Slow and Fast, 2 mA (<a href="#">Table 30</a>).</li> <li>- <math>T_{IDOCK}</math> and <math>T_{IDOCKD}</math> in <a href="#">Table 34</a>.</li> <li>- Setup/Hold for Control Lines and Data Lines in <a href="#">Table 36</a>.</li> <li>- Add <math>T_{IDELAYPAT\_JIT}</math> and revised <math>T_{IDELAYRESOLUTION}</math> in <a href="#">Table 38</a>, page 35 and added Notes 1 and 2.</li> <li>- Revised <math>T_{RCK}</math> <a href="#">page 36</a> and removed <math>T_{CKSR}</math> <a href="#">Table 39</a>, page 35.</li> <li>- Replaced <math>T_{TWC}</math> with <math>T_{MCP}</math> symbol in <a href="#">Table 40</a>, page 37.</li> <li>- Revised <math>T_{CECK}</math> in <a href="#">Table 41</a>.</li> <li>- Revised <math>T_{RCKO\_FLAGS}</math> and <math>T_{RDCK\_DI\_ECC}</math> encode only in <a href="#">Table 42</a>.</li> <li>- Revised Hold Times of Data/Control Pins to the Input Register Clock. Setup/Hold times of {PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK. Hold times of some of the CE pins. Hold times of some of the RST pins. Hold times of {A, B} input to {P, CARRYOUT} output using multiplier and {ACIN, BCIN} input to {P, CARRYOUT} output using multiplier, CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier, in <a href="#">Table 43</a>.</li> <li>- Updated and added values to <a href="#">Table 44</a>, page 43.</li> </ul> </li> <li>• Revised -1 speed <math>F_{MAX}</math> value in <a href="#">Table 46</a>, page 45.</li> <li>• Added Note 4 to <math>T_{LOCKMAX}</math> and revised <math>F_{INDUTY}</math>, <math>F_{INMAX}</math>, and <math>F_{VCOMAX}</math> in <a href="#">Table 48</a>, page 46.</li> <li>• Added <math>\pm</math> values to <a href="#">Table 52</a> and <a href="#">Table 53</a>. Changed <math>T_{OUT\_OFFSET}</math> in <a href="#">Table 53</a>.</li> <li>• In <b>Virtex-5 Pin-to-Pin Output Parameter Guidelines</b>:                         <ul style="list-style-type: none"> <li>- Revised values in <a href="#">Table 57</a> through <a href="#">Table 63</a>.</li> </ul> </li> <li>• In <b>Virtex-5 Pin-to-Pin Input Parameter Guidelines</b>:                         <ul style="list-style-type: none"> <li>- Revised values in <a href="#">Table 64</a> through <a href="#">Table 70</a>.</li> </ul> </li> <li>• In <b>ChipSync™ Source-Synchronous Switching Characteristics</b>:                         <ul style="list-style-type: none"> <li>- Revised values in <a href="#">Table 71</a>, page 66.</li> <li>- Added package skew values to <a href="#">Table 72</a>, page 67.</li> <li>- Revised values in <a href="#">Table 74</a>, page 68.</li> </ul> </li> </ul>

Date	Version	Revision
06/15/07	3.2	<ul style="list-style-type: none"> <li>• Updated <math>T_{STG}</math> in <a href="#">Table 1</a>.</li> <li>• Corrected <math>V_{OH}/V_{OL}</math> in <a href="#">Table 9</a> and <a href="#">Table 10</a>, <a href="#">page 7</a>.</li> <li>• Changed the design software version that matches this data sheet above <a href="#">Table 28</a> on <a href="#">page 21</a>.</li> <li>• Added “<a href="#">Production Silicon and ISE Software Status</a>,” <a href="#">page 22</a>.</li> <li>• Added <math>T_{IODELAY\_CLK\_MAX}</math> and revised <math>T_{CKSR}</math> in <a href="#">Table 38</a>, <a href="#">page 35</a>.</li> <li>• In <a href="#">Virtex-5 Pin-to-Pin Output Parameter Guidelines</a>: Revised values in <a href="#">Table 58</a> through <a href="#">Table 63</a>.</li> <li>• In <a href="#">Virtex-5 Pin-to-Pin Input Parameter Guidelines</a>: Revised values in <a href="#">Table 65</a> through <a href="#">Table 70</a>.</li> <li>• Corrected units to ns in <a href="#">Table 71</a>, <a href="#">page 66</a>.</li> </ul>
06/26/07	3.3	<ul style="list-style-type: none"> <li>• Added conditions to <math>DV_{PPIN}</math> in <a href="#">Table 16</a>, <a href="#">page 12</a>.</li> <li>• Changed the <math>F_{GTMAX}</math> symbol name to <math>F_{GTPMAX}</math>.</li> <li>• Updated GTP maximum line rates to 3.75 Gb/s in <a href="#">Table 18</a>, <a href="#">page 14</a>.</li> <li>• Updated maximum frequencies in <a href="#">Table 21</a>, <a href="#">page 15</a>.</li> <li>• Added 3.75 Gb/s condition and changed maximum value of <math>F_{GTX}</math> in <a href="#">Table 22</a>, <a href="#">page 15</a>.</li> <li>• Added 3.75 Gb/s sinusoidal jitter specification and changed maximum value of <math>F_{GRX}</math> in <a href="#">Table 23</a>, <a href="#">page 16</a>.</li> <li>• Changed analog input common mode ranges in <a href="#">Table 25</a>, <a href="#">page 17</a>.</li> <li>• Changed <math>T_{PKGSKEW}</math> values in <a href="#">Table 72</a>, <a href="#">page 67</a>.</li> </ul>
07/26/07	3.4	<ul style="list-style-type: none"> <li>• Added maximum value of <math>I_{REF}</math> to <a href="#">Table 3</a>, <a href="#">page 2</a>.</li> <li>• Revised <a href="#">Table 28</a> and changed the design software version in <a href="#">Table 29</a> for production devices.</li> <li>• In <a href="#">Table 38</a>, <a href="#">page 35</a>, added High Performance Mode to Note 2.</li> <li>• In <a href="#">Table 44</a>, <a href="#">page 43</a>, revised description of <math>T_{SMDCCK}/T_{SMCKD}</math>.</li> <li>• Added Note 4 to <math>T_{DUTYCYCRANGE\_200\_400}</math> frequency range in <a href="#">Table 51</a>, <a href="#">page 49</a>.</li> <li>• In <a href="#">Virtex-5 Pin-to-Pin Input Parameter Guidelines</a>: Revised note 1 in <a href="#">Table 64</a> through <a href="#">Table 69</a>.</li> </ul>
09/27/07	3.5	<ul style="list-style-type: none"> <li>• Added <math>I_{BATT}</math> value and Note 2 to <a href="#">Table 3</a>.</li> <li>• Added <b>DRP Clock Frequency</b> and Note 4 to <a href="#">Table 25</a>. Revised the typical and maximum values and units for gain error and bipolar gain error.</li> <li>• Removed unsupported XC5VSX95T -3 speed grade from <a href="#">Table 28</a> and <a href="#">Table 29</a>.</li> <li>• Removed unsupported I/O standards (LVDS_33, LVDSEXT_33, and ULVDS_25) from <a href="#">Table 25</a>. Also updated LVDSEXT, 2.5V in <a href="#">Table 33</a>.</li> <li>• Added values to <b>Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK</b> in <a href="#">Table 44</a>.</li> <li>• In <a href="#">Virtex-5 Pin-to-Pin Input Parameter Guidelines</a>: Revised note 1 in <a href="#">Table 64</a> through <a href="#">Table 70</a>.</li> </ul>
11/05/07	3.6	<ul style="list-style-type: none"> <li>• Removed note 1 from <a href="#">Table 26</a>, <a href="#">page 19</a>. <math>F_{MAX}</math> of clock is not an applicable limitation.</li> <li>• Revised DDR2 memory interface performance in <a href="#">Table 27</a>, <a href="#">page 20</a>.</li> <li>• Revised <a href="#">Table 29</a> to add ISE 9.2i SP3 where applicable.</li> <li>• Removed XC5VSX95T -3 speed grade support from applicable tables.</li> <li>• Removed unsupported I/O standard (LVPECL_33) from <a href="#">Table 32</a> and added LVPECL_25.</li> <li>• Added <math>T_{SMCO}</math> and <math>T_{SMCKBY}</math> to <a href="#">Table 44</a>, <a href="#">page 43</a>.</li> <li>• Revised note 3 in <a href="#">Table 49</a>, <a href="#">page 47</a> and <a href="#">Table 50</a>, <a href="#">page 48</a>.</li> <li>• Clarified notes in <a href="#">Table 60</a> to <a href="#">Table 63</a>, and <a href="#">Table 67</a> to <a href="#">Table 70</a>.</li> <li>• Revised note 1 in <a href="#">Table 72</a>.</li> </ul>